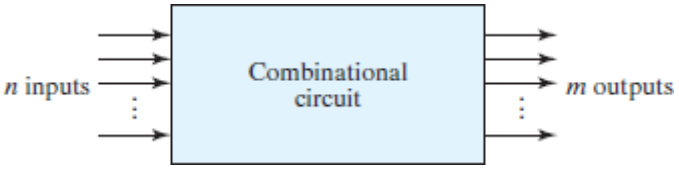
CS3351 DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

QUESTION BANK

TWO MARK QUESTIONS & ANSWERS

1) Define combinational logic. (May 2008, 2016)

A combinational circuit consists of logic gates whose outputs at any time are determined fromonly the present combination of inputs. A combinational circuit performs an operation that canbe specified logically by a set of Boolean functions.



2) What are sequential circuits?

Sequential circuits employ storage elements in addition to logic gates. Their outputs are a functionof the inputs and the state of the storage elements. Because the state of the storage elements is a function of previous inputs, the outputs of a sequential circuit depend not only on present values of inputs, but alsoon past inputs, and the circuit behavior must be specified by a time sequence of inputs and internal states.

3) Write the design procedure for combinational circuits?

The procedure involves the following steps:

1. From the specifications of the circuit, determine the required number of inputs and outputs and assigna symbol to each.
2. Derive the truth table that defines the required relationship between inputs and outputs.
3. Obtain the simplified Boolean functions for each output as a function of the input variables.
4. Draw the logic diagram and verify the correctness of the design (manually or by simulation).

4) What is half adder?

A half-adder is an arithmetic circuit block that can be used to add two bits and produce two outputs SUM and CARRY.

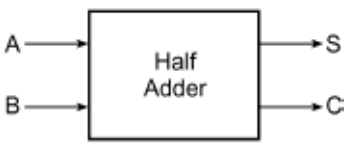
The Boolean expressions for the SUM and CARRY outputs are given by the equations

$$\text{SUM } S = A.\overline{B} + \overline{A}.B$$

$$\text{CARRY } C = A.B$$

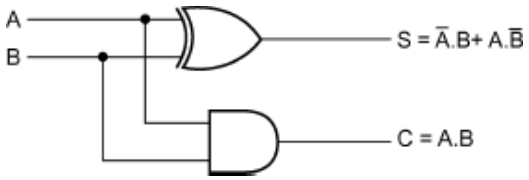
Truth Table:

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

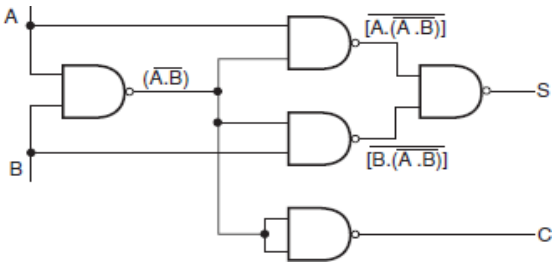


5) Draw the logic diagram of half adder using NAND gate. (May 2013)

Logic Diagram:



Half adder using NAND gate:



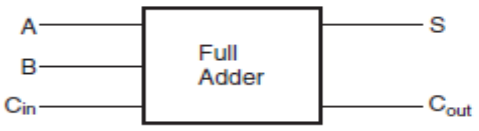
6) What is Full adder? Draw the truth table of full adder. (Apr 2018)

A Full-adder is an arithmetic circuit block that can be used to add three bits and produce two outputs SUM and CARRY.

The Boolean expressions for the SUM and CARRY outputs are given by the equations

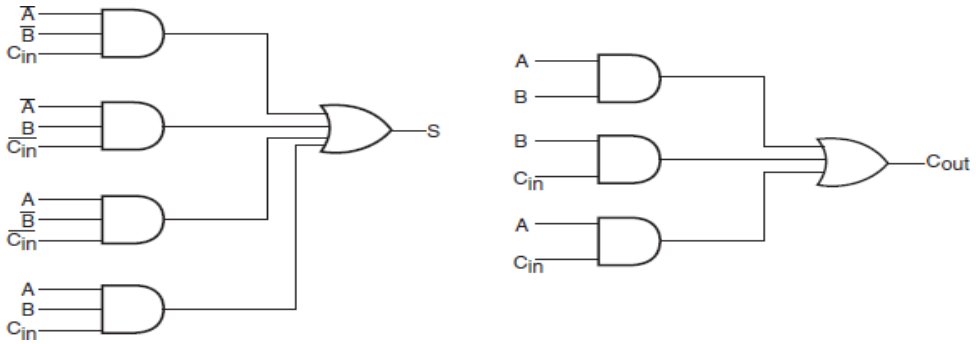
$$S = \overline{A}.\overline{B}.C_{in} + \overline{A}.B.\overline{C}_{in} + A.\overline{B}.\overline{C}_{in} + A.B.C_{in}$$

$$C_{out} = B.C_{in} + A.B + A.C_{in}$$



A	B	C_{in}	SUM (S)	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

7) Draw the Logic diagram of full adder.

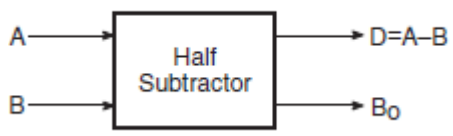


8) What is Half subtractor?

A half-subtractor is a combinational circuit that can be used to subtract one binary digit from another to produce a DIFFERENCE output and a BORROW output. The BORROW output here specifies whether a '1' has been borrowed to perform the subtraction. The Boolean expression for difference and borrow is:

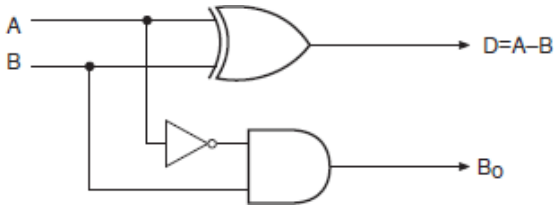
$$D = \overline{A}.B + A.\overline{B}$$

$$B_o = \overline{A}.B$$

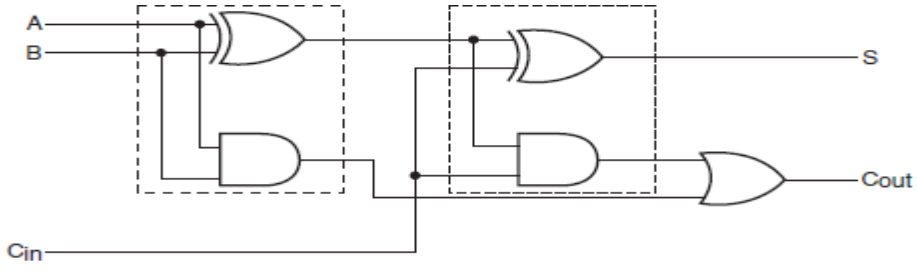


A	B	D	B_O
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

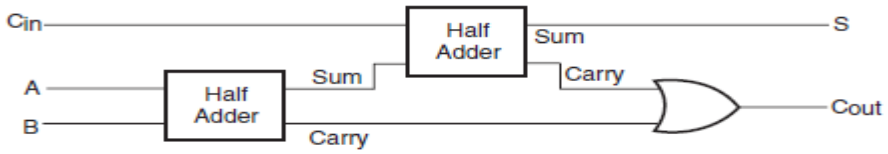
Logic diagram:



9) Draw Full adder using Two half adder. (Apr – 2019)



(a)



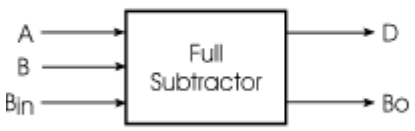
(b)

10) What is Full subtractor? Write the truth table of full subtractor. (Nov 2017)

A full subtractor performs subtraction operation on two bits, a minuend and a subtrahend, and also takes into consideration whether a '1' has already been borrowed by the previous adjacent lower minuend bit or not. As a result, there are three bits to be handled at the input of a full subtractor, namely the two bits to be subtracted and a borrow bit designated as Bin . There are two outputs, namely the DIFFERENCE output D and the BORROW output Bo. The BORROW output bit tells whether the minuend bit needs to borrow a '1' from the next possible higher minuend bit. The Boolean expression fordifference and barrow is:

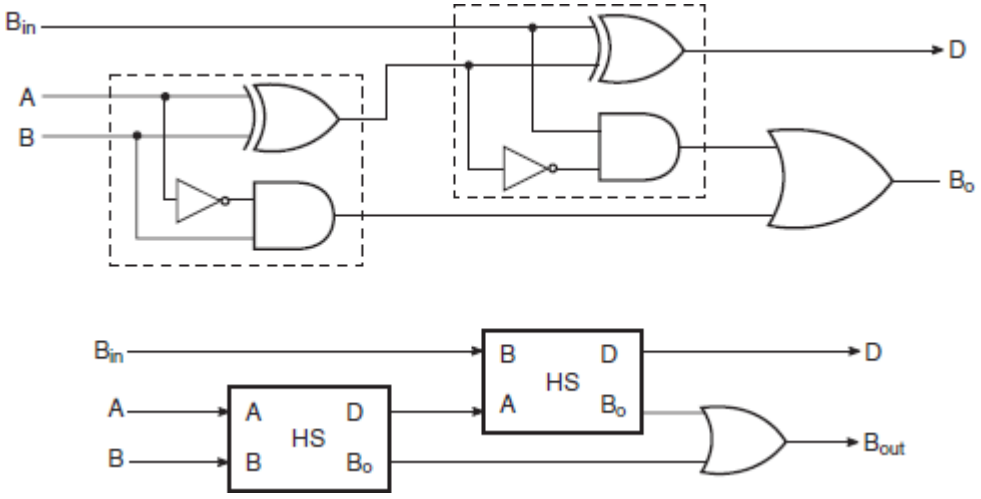
$$D = \overline{A}.\overline{B}.B_{in} + \overline{A}.B.\overline{B}_{in} + A.\overline{B}.\overline{B}_{in} + A.B.B_{in}$$

$$B_o = \overline{A}.B + \overline{A}.B_{in} + B.B_{in}$$



	Subtrahend (B)	Borrow In (B_{in})	Difference (D)	Borrow Out (B_O)
	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

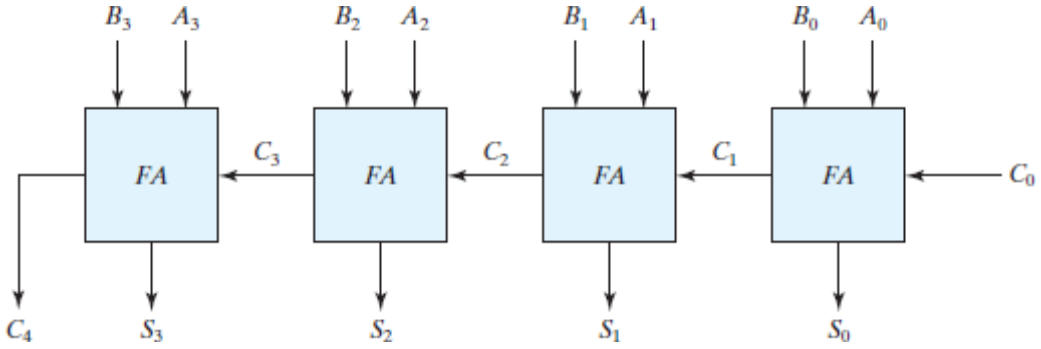
11) Draw Full subtractor using two half subtractor.



12) What is Parallel Binary Adder (Ripple Carry Adder)?

A binary adder is a digital circuit that produces the arithmetic sum of two binary numbers.It can beconstructed with full adders connected in cascade, with the output carryfrom each full adder connected to the input carry of the next full adder in the chain.

13) Draw the logic diagram for four bit binary parallel adder.



14) What is 1's complement of a number?

The 1's complement of a binary number is formed bychanging 1 to 0 and 0 to 1.

Example:

1. The 1's complement of 1011000 is 0100111.
2. The 1's complement of 0101101 is 1010010.

15) What is 2's complement of a number?

The 2's complement of a binary number is formed by adding 1 with 1's complement of a binary number.

Example:

1) The 2's complement of 1101100 is 0010100

2) The 2's complement of 0110111 is 1001001

16) How Subtraction of binary numbers perform using 2's complement addition?

✓ The subtraction of unsigned binary number can be done by means of complements.

- ✓ Subtraction of A-B can be done by taking 2's complement of B and adding it to A.
- ✓ Check the resulting number. If carry present, the number is positive and remove the carry.
- ✓ If no carry present, the resulting number is negative, take the 2's complement of result and putnegative sign.

17) Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction (a) X - Y and (b) Y - X by using 2's complements.Solution:

(c) X = 1010100

2's complement of Y = +

0111101Sum= 10010001

Discard end carry. *Answer*: X - Y = 0010001

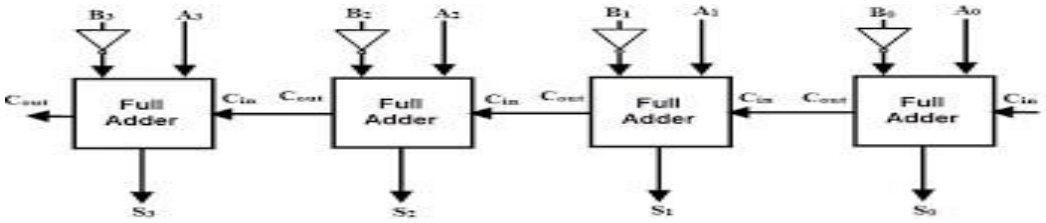
(d) Y = 1000011

2's complement of X= +

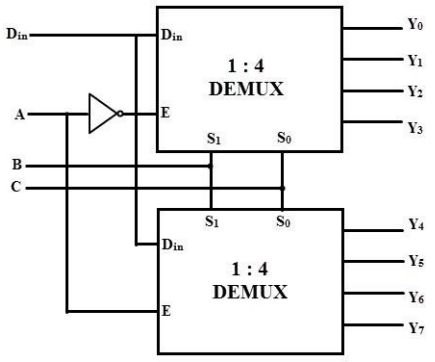
0101100Sum= 1101111

There is no end carry. Therefore, the answer is Y - X = -(2's complement of 1101111) =-0010001.

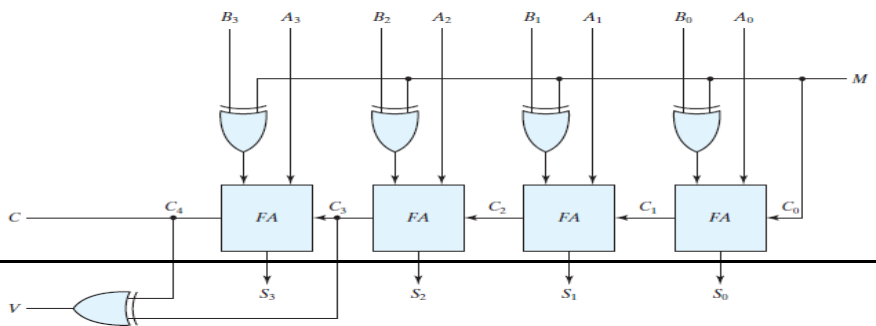
18) Draw the logic diagram of Parallel Binary Subtractor.



19) Draw 1:8 Demux using two 1:4 demux. (Nov 2018)



20) Draw the logic diagram of 2's complement adder/subtractor. (May 2013)



The mode input *M* controls the operation. When *M* = 0, the circuit is an adder, and when *M* = 1,the circuit becomes a subtractor.

21) What is Magnitude Comparator? [NOV – 2019]

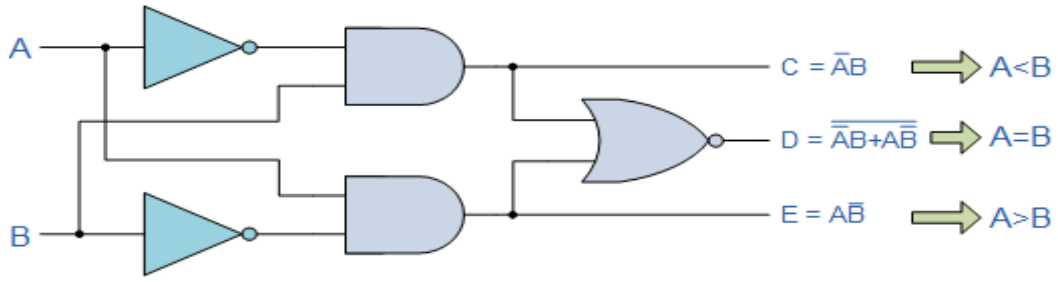
The comparison of two numbers is an operation that determines whether one number is greater than, less than, or equal to the other number. A magnitude comparator is a combinational circuit that compares two numbers A and B and determines their relative magnitudes.

The outcome of the comparison is specified by three binary variables that indicate whether A > B, A = B, or A < B.

22) Design a 1-bit Magnitude Comparator. Truth table:

Inputs		Outputs		
B	A	A > B	A = B	A < B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Logic Circuits:



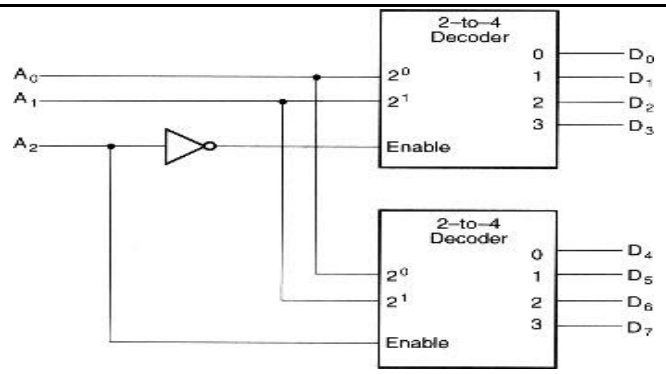
23) What is Decoder? What are binary decoders? (Nov 2017)

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. If the n -bit coded information hasunused combinations, the decoder may have fewer than 2^n outputs.

The purpose of a decoder is to generate the 2^n (or fewer) minterms of *n* input variables, shown belowfor two input variables.

24) Design a 3 to 8 decoder with 2 to 4 decoder.

Not that the two to four decoder design shown earlier, with its *enable* inputs can be used to build a three to eight decoder as follows.



25) What is Encoder? (May 2012)

An encoder is a digital circuit that performs the inverse operation of a decoder. An encoder has 2^n (or fewer) input lines and n output lines. The output lines, as an aggregate, generate the binary code corresponding to the input value.

26) What is Priority Encoder? (Apr 2017)

A priority encoder is an encoder circuit that includes the priority function. The operation of the priority encoder is such that if two or more inputs are equal to 1 at the same time, the input havingthe highest priority will take precedence.

27) Define Multiplexer (MUX) (or) Data Selector. (Dec 2006, May 2011) [NOV – 2019]

A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2^n input lines and n selection lines whose bit combinationsdetermine which input is selected.

28) What is De-multiplexer?

The de-multiplexer performs the inverse function of a multiplexer, that is it receives information on one line and transmits its onto one of 2^n possible output lines. The selection is by *n* input select lines.

29) What is Parity?

A parity bit is an extra bit included with a binary message to make the number of 1's eitherodd or even. The message, including the parity bit, is transmitted and then checked at the receiving end for errors. An error is detected if the checked parity does not correspond with the onetransmitted.

30) What is Parity Checker / Generator:

The circuit that generates the parity bit in the transmitter is called a *parity generator*. The circuit that checks the parity in the receiver is called a *parity checker.*

31) What is even parity and odd parity?

In even parity system, the parity bit is '0' if there are even number of 1s in the data and the parity bit is '1' if there are odd number of 1s in the data.

In odd parity system, the parity bit is '1' if there are even number of 1s in the data and the

parity bit is '0' if there are odd number of 1s in the data.

31) Give the applications of Demultiplexer.

i) It finds its application in Data transmission system with error detection.

ii) One simple application is binary to Decimal decoder.

32) Mention the uses of Demultiplexer.

Demultiplexer is used in computers when a same message has to be sent to different receivers. Not onlyin computers, but any time information from one source can be fed to several places.

33) Give other name for Multiplexer and Demultiplexer. Multiplexer is otherwise called as Data selector. Demultiplexer is otherwise called as Data distributor.

34) What is the function of the enable input in a Multiplexer?

The function of the enable input in a MUX is to control the operation of the unit.

35) List out the applications of decoder? (Dec 2006)

a. Decoders are used in counter system.

b. They are used in analog to digital converter.

c. Decoder outputs can be used to drive a display system.

36) What is the Application of Mux?

1. They are used as a data selector to select one output of many data inputs.
2. They can be used to implement combinational logic circuits
3. They are used in time multiplexing systems.
4. They are used in frequency multiplexing systems.
5. They are used in A/D & D/A Converter.
6. They are used in data acquisition system.

37) List out the applications of comparators?

a. Comparators are used as a part of the address decoding circuitry in computers to select aspecific input/output device for the storage of data.

b. They are used to actuate circuitry to drive the physical variable towards thereference value.

c. They are used in control applications.

38) What is carry look-ahead addition?

The speed with which an addition is performed limited by the time required forthe carries to propagate or ripple through all of the stage of the adder. One method ofspeeding up the process is by eliminating the ripple carry delay.

39) What is the Difference between Decoder & Demux.?

S.No	Decoder	Demux
1	Decoder is a many inputs to many Outputs	Demux is a single input to many outputs
2	There are no selection lines.	The selection of specific output line is controlled by the value of selection lines.

40) How Binary to Gray Code Conversion done?

Consider b1, b2, b3, b4 and b5 is the Binary Number and it is need be converted into Grey Code.

1. Write Most Significant Bit (MSB) is same as the MSB in Binary Number.

2. The second bit of the Grey code can be found by performing the Exclusive-OR (EX-OR)operation between the First and second bits of the Binary Number.

3. The Third bit of the Grey code can be found by performing the Exclusive-OR (EX-OR) operationbetween the Third and Second bits of the given Binary Number; and so on

Part B (16 marks)

1. Explain the analysis procedure. Analyze the combinational circuit the following logic diagram
2. Construct a half adder and Full adder with necessary diagrams.
3. Design a half subtractor and Full subtractor circuits
4. Explain about binary parallel / adder subtractor.
5. Design a 2 bit magnitude comparator
6. Design a 4 bit magnitude comparators
7. Design to perform BCD addition.(or) What is BCD adder? Design an adder to perform arithmeticaddition of two decimal bits in BCD
8. Explain about decoders and encoders with necessary diagrams.
9. Implement the following functions using de-multiplexer. f1 (A,B,C) = ∑m(1,5,7), f2 (A,B,C) = ∑m(3,6,7)

Unit-II

PART A (2 Marks)

1. Difference between Combinational & Sequential Circuits.

S .no	Combinational Circuits	Sequential Circuits
1	The output at all times depends only on the present combination of input variables.	The output not only depends on the present input but also depends on the past history input variables.
2	Memory unit is not Required	Memory unit is required to store the past history of input variable
3	Clock input is not needed.	Clock input is needed.

2. What are the classifications of sequential circuits?

The sequential circuits are classified on the basis of timing of their signals in to two types. They are 1)Synchronous sequential circuit.2) Asynchronous sequential circuit.

3. **Define Latch.**

The basic unit for storage is Latch. A Latch maintain its output state either at 1or 0 until directed by an input signal to change its state.

4. Define a flip flop.

A flip-flop is a storage device capable of storing one bit of information. It has two states either 0 or 1. It is also called bistable multivibrator.

5. What are the different types of flip-flop?

The various types of flip flops are 1). SR flip-flop 2). D flip-flop 3). JK flip-flop 4). T flip-flop

6. What is the main difference between a latch and flip flop?

- The output of latch changes immediately when its input changes.
- The output of a flip-flop changes only when its clock pulse is active and its input changes.
- Input changes do not affect output if its clock is not activated.

7. State few application of Flip-Flop.

- Used as a memory element.
- Used as delay elements.
- Data transfer
- Used as a building block in sequential circuits such as counters and registers.

8. What is the operation of D flip-flop?

In D flip-flop during the occurrence of clock pulse if D=1, the output Q is set and if D=0, the output is reset. Set – 1, Reset – 0.

9. What is the operation of JK flip-flop?

When K input is low and J input is high the Q output of flip-flop is set.
When K input is high and J input is low the Q output of flip-flop is reset.
When both the inputs K and J are low the output does not change
When both the inputs K and J are high it is possible to set or reset the flip-flop(ie) the output toggle onthe next positive clock edge.

10. What is the operation of T flip-flop? (Nov 2018) Page 12

T flip-flop is also known as Toggle flip-flop. 1). When T=0 there is no change in the output. 2). When T=1 the output switch to the complement state (ie) the output toggles.

11. Define race around condition.

In JK flip-flop output is fed back to the input. Therefore change in the output results change in the input. Due to this in the positive half of the clock pulse if both J and K are high then output toggles continuously. This condition is called 'race around condition'.

12. What is triggering? What is the need for trigger in flip-flop?

A flip-flop is made to change its state by application of a clock pulse after giving inputs. This is called triggering. The clock (triggering input) is given to synchronize the change in the output with it.

13. What is meant by level and edge-triggering? (Nov 2017) (Apr – 2019)

✓If flip-flop changes its state when the clock is positive (high) or negative (low) then, that flip flop is said to be *level triggering flip-flop*.

✓If the flip-flop changes its state at the positive edge (rising edge) or negative edge (falling edge) of the clock is sensitive to its inputs only at this transition of the clock then flip-flop is said to be *edge triggered flip-flop.*

14. How do you eliminate race around condition in JK flip flop. ?

Using master-slave flip-flop which consists of two flip-flops where one circuit serves as a master and the other as a slave race around condition in JK flip flop is eliminated .

15. Define rise time.

The time required to change the voltage level from 10% to 90% is known as rise time (tr).

16. Define fall time.

The time required to change the voltage level from 90% to 10% is known as falltime (tf).

17. Define skew and clock skew.

The phase shift between the rectangular clock waveforms is referred to as skew and the time delay between the two clock pulses is called clock skew.

18. Define setup time.

The setup time is the minimum time required to maintain a constant voltage levels at the excitation inputs of the flip-flop device prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip flop.

19. Define hold time.

The hold time is the minimum time for which the voltage levels at the excitation inputs must remain constant after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip flop.

20. Define propagation delay.

A propagation delay is the time required to change the output after the application of the input

21. Explain the flip-flop excitation tables for RS FF.

In RS flip-flop there are four possible transitions from the present state to theNext state. They are

1). 0→0 transition: This can happen either when R=S=0 or when R=1 and S=0.

2). 0→ 1 transition: This can happen only when S=1 and R=0.

3). 1→0 transition: This can happen only when S=0 and R=1.

4). 1→1 transition: This can happen either when S=1 and R=0 or S=0 and R=0.

22. Give some applications of clocked RS Flip-flop.

Clocked RS flip flops are used in Calculators & Computers.

It is widely used in modern electronic products.

23. What is the drawback of SR Flipflop? How is this minimized? (Apr 2018)

In SR flipflop when both S and R inputs are one it will generate a Undetermined state.This is Minimized by providing feedback path or by using JK flip flop.

24.**What is counter?**

A counter is a register (group of Flip-Flop) capable of counting the number of clock pulsearriving at its clock input.

25.What is binary counter?

A counter that follows the binary number sequence is called a binary counter.

26.State the applications of counters.

- Used as a memory Element.
- Used as a Delay Element.
- Used as a basic building block in sequential circuits such as counters and registers.
- Used for Data Transfer, Frequency Division & Counting.

27.List the types of counters.

Counter are classified into two types,

- ✓ Asynchronous (Ripple) counters.
- ✓ Synchronous counters.

28.Give the comparison between synchronous & Asynchronous counters.

S.No	Asynchronous counters	Synchronous counters
1.	In this type of counter flip-flops are connected in such a way that output of 1st flip-flop drives the clock for the next flip - flop.	In this type there is no connection between output of first flip-flop and clock input ofthe next flip – flop
2	All the flip-flops are not clocked simultaneously	All the flip-flops are clocked simultaneously
3	Logic circuit is very simple even for more number of states	Design involves complex logic circuit as number of states increases
4	Counters speed is low.	Counters speed is high.

29.State the Steps or Design procedure for Synchronous Counter.

Preparation of 1). State Diagram

2). State Table

3). State Assignment

4). Excitation Table (Consider which Memory Unit Using)

5). K-Map

6). Circuit Diagram

30.Define state diagram.

State diagram is the graphical representation of the information available in a state table. In state diagram, a state is represented by a circle and the transitions between states are indicated by directed lines connecting the circles.

31.What is the use of state diagram?

i) Behavior of a state machine can be analyzed rapidly.

ii) It can be used to design a machine from a set of specification

32.What is state table? (Nov 2018)

A stable table is a table that represents relationship between inputs, outputs and flip-flop states, is called state table. Generally it consists of four section present state, next state, input and output.

33. What is a state equation?

A state equation also called, as an application equation is an algebraic expression that specifies the condition for a flip-flop state transition. The left side of the equation denotes the next state of the flip-flop and the rightside, a Boolean function specifies the present state.

34. What do you mean by next state?

The present state and the external inputs determine the outputs and the next state of thesequential circuit.

35. Define synchronous sequential circuit.

SynchronousSequential circuits are circuits in which the signals can affect the memory elementsonly atdiscrete instant of time.

36. What are the steps for the design of asynchronous sequential circuit?

iii) Construction of primitive flow table

iv) Reduction of flow table

v) State assignment is made

vi) Realization of primitive flow table

37. Define registers.

A register is a group of flip-flops. An-bit register has a group of n flip-flops and is capable of storingany binary information/number containing n-bits.

38. Define shift registers.

A register capable of shifting its binary information in one or both directions is called as a shift register. It consists of a chain of flip flops in cascade, with the output of one flip flop

connected to the input of the next flip-flop

39. What are the different types of shift registers?[Nov 2010,April 2007,Apr 2018, Nov 2018]

a. Serial In Serial Out Shift Register
b. Serial In Parallel Out Shift Register
c. Parallel In Serial Out Shift Register
d. Parallel In Parallel Out Shift Register
e. Bidirectional Shift Register

40. State the applications of shift register.Shift registers are widely used in

- Time delay circuits
- As Serial to parallel converter
- As Parallel to serial converters
-

UNIT II
PART B (16 Marks)

1. i) Realize a JK flip flop using SR flip flop. (8)
   ii) Realize a SR flip flop using NAND gates and explain its operation. (8)
2. Explain various steps in the analysis of synchronous sequential circuits with suitable example. (16)
3. i) Distinguish between a combinational logic circuit and a sequential logic circuit (4)
   ii) Derive the characteristic equation of SR flip flop T1 PG 257. (8)
   iii) Using a JK flip flop, explain how a D flip flop can be obtained. (4)
4. Design a four state down counter using T flip flop. (16)
5. Design a 4-bit synchronous 8421 decade counter with ripple carry. (16)
6. Design a synchronous 3-bit gray code up counter with the help of Excitation table (16)
7. Describe the input and output action of JK master/slave flip flops. (16)
8. Design a MOD-10 synchronous counter using JK flip flops
9. Realize SR neither flip flop using NOR gates and explain its operation.
10. Explain the different methods of state assignment
11. State with a neat example the method for the minimization of primitive flow table.

Unit-III
PART A (2 marks)

1. **What are the five components of computer system? Apr/May 2017, 2019**

   The five classic components of computers are input unit, output unit, memory unit, arithmetic & logic unit and control unit.

2. **What is cache memory?**

   The small and fast RAM units are called as caches.

   When the execution of an instruction calls for data located in the main memory, the data are fetched and a copy is placed in the cache.

   - Later if the same data are required it reads directly from the

cache.3. **What is the function of ALU?**

- Most of the computer operations (arithmetic & logic) are performed in ALU. The data

required for the operation is brought by the processor and the operation is performed by the ALU.

4. What is the function of control unit?

- The Control unit is the main part of the computer that coordinates the entire computer operations. Data transfers between the processor and memory controlled by the control unit through timing signal.

5. What are basic operations of a computer memory?

The basic operations of the memory are READ and WRITE.

- READ – read the data from input device to memory.
- WRITE – writes data to the output device.

6. List out the operations of the computer.

The computer accepts the information in the form of programs and data through an input unit and storesit in the memory.

1. Information stored in the memory is fetched under program control into an arithmetic and logic unitwhere it is processed.
2. Processed information leaves the computer through an output unit.
3. All activities inside the machines are directed by the control unit.

7. What are the main elements of a computer?

- **Processor:** To interpret and execute programs.
- **Memory:** For storing programs and data.
- **Input-output equipment:** For transferring information between the computer and outside world.

8. Define Computer design.

- It is concerned with the hardware design of the computer. Once the computer specifications are formulated, it is the task of the designer to develop hardware for the system.
- Computer design is concerned with the determination of what hardware should be used and how the parts should be connected. This aspect of computer hardware is sometimes referred to as computer implementation.

9. What is instruction set architecture?

- An abstract interface between the hardware and the lowest level software that encompasses all theinformation necessary to write a machine language program that will run correctly.
- Including instructions, registers, memory access, I/O and so on.

10. State Amdahl's law. Nov / Dec 2014

- Amdahl's Law is used to find the execution time of a program after making the improvement. Itcan be represented in an equation as follows:

$$\text{Execution time after improvement} = \frac{\text{Execution time affected by improvement}}{Amount\ of\ improvement} + Execution\ time\ unaffected$$

- Hence, Amdahl‘s Law can be used to estimate performance improvements.

11. Define Stored Programmed Concept.

- Storing program and their data in the same high-speed memory.
- It enables a program to modify its own instructions (such self-modifying Programs haveundesirable aspects, however and are rarely used).

12. What are the registers generally contained in the processor?(Nov/Dec-2019)

- MAR – Memory Address Register.
- MDR – Memory Data Register.
- IR – Instruction Register.
- R0 – Rn – General purpose Register.
- PC – Program Counter.

13. What do you mean by Memory address register (MAR) and Memory dataregister (MDR)?

- The MAR holds the address of the location to be accessed.
- The MDR contains the data to be written into or read out of the addressed location.

14. What is Data path?

- The component of the processor that performs arithmetic operations is called data path.

15. What is elapsed time of computer system?

- The total time to execute the total program is called elapsed time.
- It is affected by the speed of the processor, the disk and the printer.

16. What is processor time of a program?

- The period during which the processor is active is called processor time of a program.
- It depends on the hardware involved in the execution of individual machine instructions.

17. Define clock rate.

- The clock rate is given by,

  R=1/P,

- Where P is the length of one clock. It can be measure as cycles per second (Hertz).

18. What is meant by clock cycle?

- Processor circuit is controlled by a timing signal called a clock.
- The clock defines regular time intervals, called clock cycle.
- To execute the machine instruction the processor divides the action to be performed intosequence of basic steps. Each step can be completed in one clock cycle.

19. Write down the basic performance equation. (Apr/May-2014)(Nov/Dec 2019)T=N*S/R

Where

T-Processor time

N-Number of machine instructions

S-Number of basic steps needed to execute one machine

instructionR-Clock rate

20. What is meant by addressing mode? List its types. (May/June 2013) Nov/ Dec 2013

The addressing mode is defined as the different ways in which the location or of an operand is specifiedin an instruction.

The different types of addressing modes are:

1. Immediate addressing mode
2. Register addressing mode
3. Direct or absolute addressing mode
4. Indirect addressing mode
5. Indexed addressing mode
6. Relative addressing mode
7. Auto increment
8. Auto decrement

21. Define Register addressing mode with an example.

- In register addressing mode, the operand is the content of a processor register. The name (address)of the register is given in the instruction.

22. List the basic instruction types. May / June 2013

The various instruction types are,

- Three address instructions
- Two-address instructions
- Single-address instructions
- Zero-address instructions

23. What is register?

- A small set of high-speed storage devices called registers, which serve as implicit storagelocations for operands and results.

24. List the phases, which are included in the each instruction cycle?

- **Fetch:** Fetches instruction from main memory (M).
- **Decode:** Decodes the instruction‘s opcode.
- **Load:** Loads (read) from M any operands needed unless they are already in CPU Registers.
- **Execute**: Executes the instruction via a register-to-register operation using an appropriatefunctional unit of the CPU such as a fixed–point adder.
- **Store:** Stores (write) the results in M unless they are to be retained in CPU register.

25. What are the types of computer?

- Mini computer
- Micro computers
- Mainframe computers

- Super computers

26. What are the two major steps in processing an instruction? (Or) Write the two steps thatare common to implement any type of instruction. Nov. / Dec. 2018

- **Fetch step:** During this step a new instruction is read from the external memory M by the CPU.
- **Execute step:** During this step operations specified by the instructions are executed bythe CPU.

27. What are the speedup techniques available to increase the performance of a computer?

- **Cache:** It is a fast accessible memory often placed on the same chip as the CPU. It is used to reduce the average time required to access an instruction or data to a single clock cycle.
- **Pipelining:** Allows the processing of several instructions to be partially overlapped.
- **Super scalar:** Allows processing of several instructions in parallel (full overlapping).

28. What are Timing signals?

- Timing signals are signals that determine when a given action is to take place.
- Data transfers between the processor and the memory are also controlled by the control unitthrough timing signals.

29. Distinguish between auto increment and auto decrement addressing mode. (May/June 2016)

Auto increment	Auto decrement
1.The effective address of the operand is the contents of the register specified in the instruction. After accessing the operand, the contents of the register are incremented to address the next location.	**1.**The contents of a register specified in the instruction are decremented and then are used as effective address to access a memory location.
2.Auto increment is symbolically represented as (Ri)+.**Example:**move(R2), R0+	**2.**Auto decrement mode is symbolically represented as -(Ri).**Example:** Move R1, -(R0)

30. Define word length. (Nov/Dec 2011)

- In computer architecture, a **word** is a unit of data of a defined bit length that can be addressed andmoved between storage and the computer processor.
- Address that is divided by 4 is called word.
- The number of bits in the word is called **word length.**
- In longer architected **word length,**the computer processor can do more in a single operation.

31. Distinguish pipelining from parallelism. (N/D2015)

- Parallelism means we are using more hardware for the executing the desired task. In parallel computing more than one processor are running in parallel. There may be some dedicated hardware running in parallel for doing the specific task.
- Parallelism increases the performance but the area also increases.
- The pipelining is an implementation technique in which multiple instructions are

overlapped inexecution.

- In case of pipelining the performance and throughput increases at the cost of pipelining registersarea.
- In pipelining there are different hazards like data hazards, control hazards etc.

32. What is the impact of frequency of clock signal applied to the microprocessor in the performance of computer? Nov/Dec 2020.

A computer's processor clock speed determines how quickly the central processing unit (CPU) can retrieve and interpret instructions. This helps your computer complete more tasks by getting them done faster. Clock speeds are measured in gigahertz (GHz), with a higher number equating to higher clock speed.

Part B(16 marks)

1. Explain in detail about the components of a computer system.
2. Explain about operations operands of computer hardware instruction. Operation of the computer hardware
3. Discuss about ISA
4. Discuss about instruction and instruction sequencing
5. What is the need for addressing in a computer system? Explain the different addressing modes with suitable examples
6. Consider the computer with three instruction classes and CPI measurements as given below and instruction counts for each instruction class for the same program from two different compilers are given. Assume that the computer's clock rate is 4 GHZ. Which code sequence will execute faster according to execution time?
7. Explain about encoding of machine instruction
8. Explain the concept of interaction between assembly and high level language.

Unit-IV

Part A (2 marks)

1. What is MIPS and write its instruction set?

MIPS is a reduced instruction set **computer** (RISC) instruction set **architecture** (ISA) developed by **MIPS** Technologies (formerly **MIPS Computer** Systems). The early **MIPS architectures** were 32-bit, with 64-bit versions added later.

MIPS instruction set:(Micro Instruction per Second)

- **The memory**-reference instructions load word (lw) and store word (sw)
- **The arithmetic**-logical instructions add, sub, AND, OR, and slt
- **The instructions-**branchequal (beq) and jump (j), which we add last.

2. What are R-type instructions? (Apr/May 2015)Nov/Dec 2020

- **op:**Basic operation of the instruction, traditionally called the **opcode**.
- **rs:**The first register source operand.
- **rt:**The second register source operand.
- **rd:**The register destination operand. It gets the result of the operation.
- **shamt:**Shift amount.
- **funct:** Function. This field, often called the *function code*, selects the specific variant of the operation in the op field.

3. Define Branch target address.

- The address specified in a branch, which becomes the new program counter (PC) if the branch is taken. In the MIPS architecture the branch target is given by the sum of the offset field of the instruction and the address of the instruction following the branch.

4. Define the terms Data path element, CPU Data path and Data path cycle? Nov / Dec 2016, Apr. / May 2018 Nov/Dec 2020.

- A unit used to operate on or hold data within a processor. In the MIPS implementation, the data path elements include the instruction and data memories, the register file, the ALU and adders.
- The path that data follows within the CPU, along buses from registers to ALU and back is called the **CPU Datapath**.
- Everything a computer does, whether playing an MPEG file, or a video game, is, in the end, essentially a sequence of very primitive operations whereby data is moved from registers to the ALU, operations are performed on that data, and then the result is returned to the registers. A single round of Registers -> ALU -> Registers is called a **CPU Datapath Cycle**.

5. When will the instruction have die effect?

- Sometime an instruction changes the contents of a register other than the destination. An instruction that uses an auto increment or auto decrement addressing mode is an example.
- Add with Carry R2, R4
- This instruction will take the carry value present in the condition code register. So it refers the register which is not represented in the instruction

6. Define branch penalty.

- The time lost as a result of a branch instruction is often referred to as the branch penalty. This will cause the pipeline to stall. So we can reduce branch penalty by calculating the branch address in early stage.

7. What is the use of instruction queue in pipeline?

- Many processors can fetch the instruction before they are needed and put them in queue is called instruction queue. This instruction queue can store several instructions.

8. Define dispatch unit.

- It is mainly used in pipeline concept. It takes the instruction from the front of the instruction queue and sends them to the execute unit for execution.

9. What is meant by branch folding and what is the condition to implement it?

- The instruction fetch unit has executed the branch instruction concurrently with in the execution of other instructions is called branch folding.
- This occurs only if at the time of branch is encountered at least one instruction is available in the queue than the branch instruction.

10. What is meant by delay branch slot?

- A location following branch instruction is called as branch delay slot. There may be more than one branch delay slot, depending on the execution time.
- The instruction in the delay slot is always fetched and at least partially executes before the branch decision is made.

11. Define delayed branching.

- It is a technique by using it we can handle the delay branch slot instructions. We can place some useful instruction in the branch delay slot and execute these instruction s when the processor is executing the branch instruction.
- If there is no useful instruction in the program we can simply place NOP instruction in delay slot. This technique will minimize the branch penalty.

12. Define branch prediction.Nov / Dec 2015

It is a technique used for reducing branch penalty associated with the condition branches. Assume that the branch will not take place and to continue the fetch instructions in sequential address order until the branch condition is evaluated.

13. What are the two types of branch prediction technique available?

The two types of branch prediction techniques are

- Static branch prediction
- Dynamic branch prediction

14. Define static and dynamic branch prediction.

- The branch prediction decision is always the same for every time a given instruction is executed.This is known as static branch prediction.
- Another approach in which the prediction may change depending on execution history is called dynamic branch prediction.

15. List the two states in the dynamic branch prediction.

- LT : Branch is likely to be taken.
- LNT : Branch is likely not to be taken.

16.List out the four stages in the branch prediction algorithm.

- ST :Strongly likely to be taken
- LT :Likely to be taken
- LNT :Likely not to be taken
- SNT :Strongly not to be taken

17. Define Register renaming. (Nov/Dec 2009)

- When temporary register holds the contents of the permanent register, the name of permanent register is given to that temporary register is called as **register renaming**.
- **For example**, if I2 uses R4 as a destination register, then the temporary register used in step TW2 is also referred as R4 during cycles 6 and 7 that temporary register used only for instructions that follow I2 in program order.
- For example, if I1 needs to read R4 in cycle 6 or 7, it has to access R4 though it contains unmodified data be I2.

18. What is pipelining and what are the advantages of pipelining? (Apr/May 2010) Nov / Dec 2013

- Pipelining is process of handling the instruction concurrently.
- The pipelining processor executes a program by one after another.

Advantages: May / June 2016

- Pipelining improves the overall throughput of an instruction set processor.
- It is applied to design of complex data path units such as multiplexers and floating points adders.

19. Name the four stages of pipelining. (Or)What are the steps in pipelining processor?

Fetch	:	Read the instruction from the memory.
Decode	:	Decode the instruction and fetch the source operands.
Execute	:	Perform the operation specified by the instruction
Write	:	Store the result in the destination location.

20. Write short notes on instruction pipelining.

- The various cycles involved in the instruction cycle.
- These fetch, decode and execute cycles for several instructions are performed simultaneously to reduce overall processing time.
- This process is referred as **instruction pipelining.**

21. What is the role of cache in pipelining? (Or) What is the need to use the cache memory in pipelining concept?(Nov/Dec 2011)

- Each stage in a pipeline is expected to complete its operation in one clock cycle. But the accessing time of the main memory is high.
- So it will take more than one clock cycle to complete its operation. So we are using cache memory for pipelining concept.
- The accessing speed of the cache memory is very high.

22. What is meant by bubbles in pipeline? Or what is meant by pipeline bubble? Nov / Dec 2016

- Any condition that causes the pipeline to be idle is known as pipeline stall. This is also known as bubble in the pipeline. Once the bubble is created as a result of a delay, a bubble moves down stream until it reaches the last unit.

23. What are the major characteristics of pipeline?

- Pipelining cannot be implemented on a single task, as it works of splitting multiple tasks into a number of subtasks and operating on them simultaneously.
- The speedup or efficiency is achieved by using a pipeline depends on the number of pipe stages and the number of available tasks that can be subdivided.

24. Give the features of the addressing mode suitable for pipelining. (Apr/May 2014)

- They access operand from memory in only one cycle.

- Only load and store instruction are provided to access memory.
- The addressing modes used do not have side effects.(When a location other than one explicitly named in an instruction as the destination operand is a affected, the instruction is said to have a side effect).
- Three basic addressing modes used do not have these features are register, register indirect and index. The first two require bus address computation. In the index mode, the address can be computed in one cycle, whether the index value is given in the instruction or in registration.

25. What is the ideal CPI of a pipelined processor?

The ideal CPI on a pipelined processor is almost always 1. Hence, we can compute the pipelined CPI:

CPI pipelined = Ideal CPI + Pipeline stall clock cycles per instruction = 1 + Pipeline stall clock cycles per instruction

26. Define Hazard and State different types of hazards that occur in pipeline.

In the domain of central processing unit (CPU) design, **hazards** are problems with the instruction pipeline in CPU microarchitectures when the next instruction cannot execute in the following clock cycle, and can potentially lead to incorrect computation results.

The various pipeline hazards are:

- Structural hazards
- Data or Data dependent hazards
- Instruction or control hazards

27. What is structural hazard?(Nov/Dec 2008) (Apr /May 2014)

- When two instructions require the use of a given hardware resource at the same time this hazard will occur. The most common case of this hazard is memory access.

28. What is data hazard in pipelining? (Nov/Dec 2007, 2008)

- A data hazard is any condition in which either the source or the destination operands of an instruction are not available at the time expected in pipeline. As a result some operation has be delayed and the pipeline stalls.
- Arise when an instruction depends on the results of a previous instruction in a way that is exposed by overlapping of instruction in pipeline

29. What are instruction hazards (or) control hazards?

- They arise while pipelining branch and other instructions that change the contents of program counter.
- The simplest way to handle these hazards is to stall the pipeline stalling of the pipeline allows few instructions to proceed on completion while stopping the execution of those which results in hazards.

30. How can we eliminate the delay in data hazard?

- In pipelining the data can be executed after the completion of the fetch operation. The data are available at the output of the ALU once the execute stage completes.
- Hence the delay can be reduced if we arrange for the result of fetch instruction to be forwarded directly for use in next step. This is known as operand forwarding.

Part B (16 Marks)

1. Briefly explain about Basic MIPS Implementation
2. Give detail description about Building a Data path. (or) Build a suitable Data path For branch instruction. Explain all the blocks with suitable example
3. Briefly explain about Control Implementation scheme
4. Give detail description about the Design of Main Control Unit.
5. Explain a 4-stage instruction pipeline. Explain the issues affecting pipeline performance. (Or) Discus the basic concepts of pipelining
6. Explain about Pipeline Performance. (Or) How to measure the performance of a pipeline? (Or)List the key aspects in gaining the performance in pipelined systems or Explain the difference types of pipeline hazards with suitable examples.
7. Discuss the modified data path to accommodate pipelined executions with a diagram
8. Explain the hazards caused by unconditional branching statements.
9. Explain about Branch prediction Algorithm
10. Explain about Conditional Branches

Unit V

1. What is Memory?

- Memory is a device used to store the data and instructions required for any operation.

2. What is the secondary memory?

- Secondary memory is where programs and data are kept on a long-term basis. Common secondary storage devices are the hard disk and optical disks. The hard disk has enormous storage capacity compared to main memory. The hard disk is usually contained inside the case of a computer.

3. What are some examples of secondary storage device?

- Some other examples of secondary storage technologies are flash memory (e.g. USB flash drives or keys), floppy disks, magnetic tape, paper tape, punched cards, standalone RAM disks, and Iomega Zip drives.

4. What are the characteristics of a secondary storage device?

- Characteristics of a secondary storage devices are,
- Capacity
- Speed
- Portability
- Durability
- Reliability

5. What are the three main categories of secondary storage?

Currently the most common forms of secondary storage device are:

- Floppy disks
- Hard disks
- Optical Disks
- Magnetic Tapes
- Solid State Devices

6. What is Bandwidth?

- The maximum amount of information that can be transferred to or from the memory per unit time is called bandwidth.

7. Define a Cache.

- It is a small fast intermediate memory between the processor and the main memory.

8. What is Cache Memory?

- Cache memory is a very high speed memory that is placed between the CPU and primary or main memory.
- It is used to reduce the average time to access data from the main memory.
- The cache is a smaller and faster memory which stores copies of the data from frequently used main memory locations.
- Most CPUs have different independent caches, including instruction and data.

9. Give the mapping techniques of cache.

The three different types of mapping techniques used for the purpose of cache memory are as follow,

- ✓ Direct Mapping
- ✓ Associative Mapping
- ✓ Set-Associative Mapping

10. What is Write Stall?

- When the processor must wait for writes to complete during write through, the processor caches is said to write stall.

11. Define Mapping Functions.

- The correspondence of memory blocks in cache with the memory blocks in the main memory is defined as mapping functions.

12. What is Address Translation?

- The conversion of virtual address to physical address is termed as address translation.

13. What is the transfer time?

- The time it takes to transmit or move data from one place to another.
- It is the time interval between starting the transfer and the completion of the transfer.

(Or)

- Transfer time is the time it takes to transfer a block of bits, typically a sector under the read / write head.

14. What is latency and seek time?

- **Seek Time** is measured defines the amount of time it takes a hard drive's read/write head to find the physical location of a piece of data on the disk.
- **Latency** is the average time for the sector being accessed to rotate into position under a head, after a completed seek.

15. What is the clock cycle time?

- The speed of a computer processor, or CPU, is determined by the clock cycle, which is the amount of time between two pulses of an oscillator.
- Computer processors can execute one or more instructions per clock cycle, depending on the type of processor.

16. What is Access Time?

- The time a program or device takes to locate a single piece of information and make it available to the computer for processing. *DRAM (dynamic random access memory)* chips for personal computers have access times of 50 to 150 nanoseconds (billionths of a second).

17. What is meant by disk fragmentation?

- Fragmentation refers to the condition of a disk in which files are divided into pieces scattered around the disk.
- It occurs naturally when you use a disk frequently, creating, deleting, and modifying files.
- At some point, the operating system needs to store parts of a file in noncontiguous clusters.

18. What is the average access time for a hard disk?

- Disk access times are measured in milliseconds (thousandths of a second), often abbreviated as ms.
- Fast hard disk drivesfor personal computers boast access times of about 9 to 15 milliseconds.
- Note that this is about 200 times slower than average DRAM.

19. What is rotational latency time?

- The amount of time it takes for the desired sector of a disk (i.e., the sector from which data is to be read or written) to rotate under the read-write heads of the disk drive.
- It is also called as rotational delay.

20. What is meant by disk latency?

- Disk latency refers to the time delay between a request for data and the return of the data. It sounds like a simple thing, but this time can be critical to the performance of a system.

21. Define Page Fault.

- If the processor access for the particular page in main memory and if the page is not present there then it is known as page fault.

22. Define a Cache Unit.

- When the CPU refers to memory and finds a required word in cache it is termed as cache hit.

23. Define Hit Ratio.(Nov/Dec 2019)Nov/Dec 2021

- The ratio of the number of hits divided by the total CPU references to memory is the hit ratio.

24. Define a Miss.Nov/Dec 2021

- When the CPU refers to memory and if the required word is not found in cache it is termed as miss.

25. What is meant by memory stall cycles? (M 2016)

- The number of cycles during which the CPU is stalled waiting for a memory access is called memory stall cycles.

26. What is Miss Penalty?

- The number of stall cycles depends on both the number of misses and the cost per miss, which is called the miss penalty.

27. Write the formula to calculate average memory access time. (Or) Write the formula to measure average memory access time for memory hierarchy performance. (Nov / Dec 2018)

- Average memory access time = Hit time + Miss rate x Miss penalty

28. What is a miss in a cache? (Or) What does Cache Miss mean? (Or) Define Cache Miss. (Nov/Dec 2010, April/May 2018)

- Cache miss is a state where the data requested for processing by a component or application is not found in the cache memory.
- It causes execution delays by requiring the program or application to fetch the data from other cache levels or the main memory.

29. Define Cache Hit. (Or) What does Cache Hit mean? (April/May 2018)

- A cache hit is a state in which data requested for processing by a component or application is found in the cache memory.
- It is a faster means of delivering data to the processor, as the cache already contains the requested data.

30. Differentiate between Cache Miss and Cache Hit.

- The difference between the two is the data requested by a component or application in a cache memory being found or not.
- In a cache miss, the data is not found so the execution is delayed because the component or application tries to fetch the data from main memory or other cache levels.
- In a cache hit, the data is found in the cache memory making it faster to process.
- The **cache *hit*** is when you look something up in a cache and it *was* storing the item and is able to satisfy the query.

31. What is miss penalty for a cache?

- Cache is a small high-speed memory. Stores data from some frequently used addresses (of main memory). Processor loads data from M and copies intocache.
- This results in extra delay, called miss penalty.
- Hit ratio = percentage of memory accesses satisfied by the cache.

32. What is miss rate in cache?

- The fraction or percentage of accesses that result in a hit is called the hit rate.
- The fraction or percentage of accesses that result in a miss is called the miss rate.

- It follows that hit rate + miss rate = 1.0 (100%).
- The difference between lower level access time and cache access time is called the miss penalty.

33. What is hit time in cache?

- AMAT's three parameters hit time (or hit latency), miss rate, and miss penalty provide a quick analysis of memory systems.
- Hit latency (H) is the time to hit in thecache. Miss rate (MR) is the frequency of cache misses, while average miss penalty (AMP) is the cost of a cache miss in terms of time.

34. How is cache memory measured?

- The CPU cache is a piece of hardware which reduces the access time to the data in the memory by keeping some part of the frequently used data of the main memory in itself.
- It is smaller and faster than the main memory.

35. What is the memory cycle time?

- Cycle time is the time, usually measured in nanosecond s, between the start of one random access memory (RAM) access to the time when the next access can be started.
- Access time is sometimes used as a synonym (although IBM deprecates it).

36. What is the memory access time?

- Memory access time is how long it takes for a character in memory to be transferred to or from the CPU.
- In a PC or Mac, fast RAM chips have an access time of 70 nanoseconds (ns) or less.
- SDRAM chips have a burst mode that obtains the second and subsequent characters in 10 ns or less.

37. What is the data transfer rate?

- The speed with which data can be transmitted from one device to another.
- Data rates are often measured in megabits (million bits) or megabytes (million bytes) per second.
- These are usually abbreviated as Mbps and MBps, respectively. Another term for data transfer rate is throughput.

38. What does access time measure?

- The total time it takes the computer to read data from a storage device such as computer memory, hard drive, CD-ROM or other mechanism.
- Computer access time is commonly measured in nanoseconds or milliseconds and the lower the access the time the better.

39. List the method to improve the cache performance.

Improving the cache performance following methods are used:

- Reduce the miss rate.
- Reduce the miss penalty.
- Reduce the time to hit in the cache.

40. What is Split Transactions?

- With multiple masters, a bus can offer higher bandwidth by using packets, as opposed to holding the bus for the full transaction. This technique is called split transactions.

41. What is Cylinder?

- Cylinder is used to refer to all the tracks under the arms at a given points on all surfaces.

42. What is Synchronous Bus?

- Synchronous bus includes a clock in the control lines and a fixed protocol for sending address and data relative to the clock.

43. Explain difference between latency and throughput.

- Latency is defined as the time required processing a single instruction, while throughput is defined as the number of instructions processes per second.

44. What is called Pages?

- The address space is usually broken into fixed-size blocks, called pages. Each page resides either in main memory or on disk.

45. What are the techniques to reduce hit time?

The techniques to reduce hit time are:

- Small and simple cache: Direct mapped.
- Avoid address translation during indexing of the cache.
- Pipelined cache access.
- Trace cache.

46. What are the categories of cache miss? (April/May 2013) (Or) Point out one simple technique used to reduce each of the three "C" misses in cache memories. (Nov/Dec 2017)

- Categories of cache misses are,
  - ✓ Compulsory
  - ✓ Capacity
  - ✓ Conflict

47. How the conflicts misses are divided? (Nov/Dec 2016)

Four divisions of conflict misses are:

- **Eight way:** Conflict misses due to going from fully associative to eight way associative.
- **Four way:**Conflict misses due to going from eight way associative to four way associative.
- **Two way:** Conflict misses due to going from four way associative to two way associative.
- **One way:** Conflict misses due to going from two way associative to one way associative.

48. What is Sequence Recorded?

- The sequence recorded on the magnetic medics is a sector number, a gap, the information for that sector including error correction cede, a gap, the sector number of the next sector and so on.

49. Write the formula to calculate the CPU execution time.

- CPU execution time = (CPU clock cycles + Memory stall cycles) x Clock cycle time.

50. Write the formula to calculate the CPU time.

- CPU time = (CPU execution clock cycles + Memory stall clock cycles) x Clock cycle time.

Part B (16 marks)

1. Explain about the memory concepts and hierarchy. What is Memory?
2. Explain about the memory management
3. Discuss in detail about various cache mapping techniques
4. Discuss the concept of virtual memory and explain how a virtual memory system is implemented, pointingout the hardware and software support
5. Discuss the concept of Programmed I/O. Discuss about Programmed I/Os associated with computers.