EC3352 VLSI AND CHIP DESIGNL T P C 3 0 0 3

OBJECTIVES:

- Study the fundamentals of CMOS circuits and its characteristics
- Learn the design and realization of combinational & sequential digital circuits.
- Architectural choices and performance tradeoffs involved in designing and realizing the circuits in CMOS technology are discussed
- Learn the different FPGA architectures and testability of VLSI circuits.

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UNIT I – MOS TRANSISTOR PRINCIPLE
MOS logic families (NMOS and CMOS), Ideal and Non Ideal IV Characteristics, CMOS devices. MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, Technology Scaling, power consumption
UNIT II COMBINATIONAL LOGIC CIRCUITS
Propagation Delays, stick diagram, Layout diagrams, Examples of combinational logic design, Elmore's constant, Static Logic Gates, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.
UNIT III SEQUENTIAL LOGIC CIRCUITS AND CLOCKING STRATEGIES
Static Latches and Registers, Dynamic Latches and Registers, Pipelines, Nonbistable Sequential Circuits. Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design
UNIT IV INTERCONNECT , MEMORY ARCHITECTURE AND ARITHMETIC CIRCUITS
Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Sequential digital circuits: adders, multipliers, comparators, shift registers. Logic Implementation using Programmable Devices (ROM, PLA, FPGA), Memory Architecture and Building Blocks, Memory Core and Memory Peripherals Circuitry
UNIT V ASIC DESIGN AND TESTING
Introduction to wafer to chip fabrication process flow. Microchip design process & issues in test and verification of complex chips, embedded cores and SOCs, Fault models, Test coding. ASIC Design Flow, Introduction to ASICs, Introduction to test benches, Writing test benches in Verilog HDL, Automatic test pattern generation, Design for testability, Scan design: Test interface and boundary scan.

OUTCOMES:

- Realize the concepts of digital building blocks using MOS transistor.
- Design combinational MOS circuits and power strategies.
- Design and construct Sequential Circuits and Timing systems.
- Design arithmetic building blocks and memory subsystems.
- Apply and implement FPGA design flow and testing.

TEXT BOOKS:

1. Neil H.E. Weste, David Money Harris ―CMOS VLSI Design: A Circuits and Systems Perspective‖, 4th Edition, Pearson , 2017 (UNIT I,II,V)
2. Jan M. Rabaey ,Anantha Chandrakasan, Borivoje. Nikolic, ‖Digital Integrated Circuits:A Design perspective‖, Second Edition , Pearson , 2016.(UNIT III,IV)

REFERENCES:

1. M.J. Smith, ―Application Specific Integrated Circuits‖, Addisson Wesley, 1997
2. Sung-Mo kang, Yusuf leblebici, Chulwoo Kim ―CMOS Digital Integrated Circuits:Analysis & Design‖,4th edition McGraw Hill Education,2013
3. Wayne Wolf, ―Modern VLSI Design: System On Chip‖, Pearson Education, 2007 R.Jacob Baker, Harry W.LI., David E.Boyee, ―CMOS Circuit Design, Layout and Simulation‖, Prentice Hall of India 2005.

UNIT I PART A(2 marks)

1. What are the advantages CMOS technology?
   - Low power consumption
   - High performance
   - Scalable threshold voltage
   - High noise margin
   - Low output drive current

2. Distinguish between nMOS and pMOS devices.

nMOS	**pMOS**
In nMOS, electrons are the majority carriers. When positive voltage is applied on gate, no. of electrons will increase. So conductivity of channel is increased	In pMOS, majority carriers are holes.
Switching speed is high, since the mobility of electron is high.	Switching speed is low, since the mobility of hole is low.
nMOS conducts at logic 1.	pMOS conducts at logic 0.

3. **What is meant by body effect?**
   V_t is not constant with respect to voltage difference between substrate and source of transistor. This is known as body effect. It is otherwise known as substrate-bias effect.

4. **What is velocity saturation?**
   The saturation current increases less than quadratically with increasing V_{gs} .Tis is caused by two effects velocity saturation and mobility degradation. At high electric fields strengths V_{ds}/L carrier velocity ceases to increase linearly with field strength. This is called velocity saturation and results in lower I_{ds} ,than expected at high V_{ds}.

5. **Define inversion layer.**
   When a higher positive potential greater than critical threshold is applied, it attracts more positive charge to the gate. These holes are repelled further and a small number of free electrons in the body are attracted to the region beneath the gate. This
   conductive layer of electrons in the p-type body is called inversion layer.

6. **Define Noise Margin.**
   Noise margin represents the amount of noise voltage on the input of a gate so that the output. will not be corrupted. It is closely relating to the dc characteristics and it is also known as noise immunity.
   There are two parameters
   - Low noise margin-NM_L
     High noise margin-NM_H

7	**What is CMOS technology?** Complementary Metal Oxide Semiconductor (CMOS) in which both n-channel MOS and p- channel MOS are fabricated in the same IC.
8	**What are the advantages of CMOS over NMOS technology?** • In CMOS technology the aluminum gates of the transistors are replaced by poly silicon gate. • The main advantage of CMOS over NMOS is low power consumption. In CMOS technology the device sizes can be easily scalable than NMOS.
9	**What are the advantages of CMOS technology?** • Low power consumption • High performance • Scalable threshold voltage • High noise margin • Low output drive current
10	**What are the disadvantages of CMOS technology?** • Low resistance to process deviations and temperature changes • Low switching speed at large values of capacitive loads
11	**What are the system approaches to prevent latch-up?** By using proper grounding technique By using decoupling capacitors at the supply pins of the IC By placing a reversed-biased diode between each supply rail and the I/O pins By placing series resistance to limit the fault current to a safe value Carefully protect electrostatic protection devices associated with I/O pads with guard rings
12	**Mention MOS transistor characteristics.** Metal Oxide Semiconductor is a three terminal device having source, drain and gate. The resistance path between the drain and source is controlled by applying a voltage to the gate. The normal conduction characteristics of an MOS transistor can be categorized as Cut off region, Non-saturated region and saturated region.
13	**What is threshold voltage?** It is defined as the minimum voltage at which the device starts conduction (ie.,) turns on.
14	**What are the different operating modes of MOS transistor?** • Accumulation mode • Depletion mode • Inversion mode
15	**What is saturated region?** Channel is strongly inverted and the drain current flow is ideally independent of drain-source voltage is called saturated region. $0<V_{gs}-V_t<V_{ds}$
16	**What are the functional parameters of threshold equation?** • Gate conductor material • Gate insulator material • Gate insulator thickness- channel doping • Impurities at the silicon- insulator interface • Voltage between the source and the substrate, Vsb
17	**What is body effect?** The threshold voltage Vt is not constant with respect to voltage difference between source and substrate is called body effect.
18	**What is channel length modulation?** The increase of the depletion layer width at the drain as the drain voltage is increased.

	This leads to a shorter channel length and an increased current is called Channel length modulation in a MOS.
19	**What is mobility variation?** The mobility is defined as the ratio of average carrier drift velocity to the electric field intensity.
20	**Define scaling?** Scaling of MOS transistor is concerned with systematic reduction of overall dimensions of the devices as allowed by the available technology, while preserving the geometric ratios found in the larger devices.
	PART B(13 marks)
1	**Explain the operation of a CMOS inverter clearly indicating the various regions of operation. (13M)** CMOS Inverter- Diagram-Circuit-Operation- input -0‖- Output -01 (2M) CMOS Inverter DC Characteristics- Cut off- Ids=0, Vgs≤ Vt –Saturated-0<Vgs-Vt<Vds - Non-Saturated-0<Vds<Vgs-Vt (3M) CMOS Inverter DC transfer and operating regions- Diagram-Region A-Region B-Region C-Region D-Region E (8M)
2	**Explain in detail about the ideal I-V characteristics and non-ideal I-V characteristics of NMOS and PMOS devices and derive its equation.(13M)** **MOS DC Equations-** Cut-off mode- Non-saturated or Linear mode- Saturated mode (4M) Non ideal IV characteristics (9M)
3	**Explain the electrical properties of MOS transistor in detail (13M)** Electrical Properties- Threshold Voltage- Threshold voltage equations-Body effect (2M) MOS DC Equations- Cut off- Ids=0, Vgs≤ Vt –Saturated-0<Vgs-Vt<Vds -Non-Saturated- 0<Vds<Vgs-Vt (2M) Small Signal AC Characteristics-Voltage gain-Figure of merit (2M) MOS Capacitances-Simple MOS capacitance model-Detailed MOS Capacitance model- MOS Device Capacitance (2M) MOS Resistance-Resistance of Non-rectangular Regions-Contact and via Resistance-Distributed RC effect-Wire length Design Guide- (1M) Inductance- Non-Ideal I-V Characteristics of MOS-Threshold voltage- Body effect- Sub threshold conduction- Channel length modulation- Mobility variation- Drain punch through- Impact ionization- Drain induced barrier lowering- Tunneling-Velocity saturation and mobilitydegradation- Junction leakage- Temperature dependence-Geometry Dependence (4M)
4	**Explain in detail about the scaling concept of CMOS chips.(13M) (May/June2013)** **Constant field Scaling-**Largest reduction in power delay product of single transistor (3M) **Constant voltage scaling-**Voltage compatibility with older circuits (3M) **Comparison of the effect of scaling on MOSFET devices-** Gate length- Gate width- Field- Oxide Thickness- Substrate doping- Gate capacitance-Oxide capacitance- Transit time- Transit frequency- Voltage- Current- Power- Power-delay (7M)
5	**Explain the operation of a CMOS inverter clearly indicating the various regions of operation. (13M)** CMOS Inverter- Diagram-Circuit-Operation- input —0‖- Output —1 (2M) CMOS Inverter DC Characteristics- Cut off- Ids=0, Vgs≤ Vt –Saturated-0<Vgs-

	Vt<Vds - Non-Saturated-0<Vds<Vgs-Vt (3M) CMOS Inverter DC transfer and operating regions- Diagram-Region A-Region B-Region C-Region D-Region E (8M)
	UNIT II(2 marks)
1	**What are the short falls of pass transistor logic?** The short fall associated with PTL is threshold variation (or) threshold drop. An NMOS device is effective at passing a 0, but it is poor at pulling a node to VDD. When the pass-transistor pulls a node high, the output only charges to VDD − Vtn. The output voltage will also gets affected when the source-to-body voltage is present (body effect).
2	**What is complementary pass transistor logic?** CPL is an alternative structure to eliminate threshold variation. The main concept behind CPL is the use of only an nMOS network for the implementation of logic functions. This results in low input capacitance and high speed operation. It consists of nMOS pass transistor logic network driven by two sets of complementary inputs and CMOS inverter used as buffers.
3	**What is swing-restored pass transistor logic?** It is an alternate configuration for PTL to eliminate threshold drop. In SRPL the output inverters are cross- coupled like a latch structure, which performs both swing restoration and output buffering.
4	**What is pass transistor logic?** It is a MOS transistor, in which gate is driven by a control signal, the source (out), the drain of the transistor is called constant or variable voltage potential (in). When the control signal is high, input is passed to the output and when the control signal is low, the output is in high impedance (floating).
5	**Write the application of TG.** • Multiplexing element or path selector • A latch element • An Analog switch • Act as a voltage controlled resistor connecting the input and output.
6	**List the Important properties of static CMOS design.** • At any instant of time, the output of the gate is directly connected to *VSS* or *VDD*. • All functions are composed of either AND‘ed or OR‘ed sub functions. The AND function is composed of NMOS transistors in series. The OR function is composed of NMOS transistors in parallel. • Contains a pull-up network (PUP) and pull down network (PDN). • PUP networks consist of PMOS transistors. • PDN networks consist of NMOS transistors. • Each network is the dual of the other network. The output of the complementary gate is inverted
7	**What are the advantages of multiple threshold transistors?** The threshold problem in pass transistors can be reduced using multiple threshold transistors. The primary goal of multiple threshold voltage circuits is to selectively scale the threshold voltages together with the supply voltage in order to enhance speed without increasing the subthreshold leakage current.
8	**List the limitations of static CMOS design.** The main limitation of static circuits is slower speed as compared to dynamic circuits. The reasons are

	• Increased gate capacitance due to the presence of both PMOS and NMOS transistors • Output depends on the previous cycle inputs due to charges that may be present at internal inputs. Multiple switching of the output within a cycle depending on the input switching pattern.
9	**Define logical effort.** Logical effort of a gate is defined as the ratio of the input capacitance of the gate to the input capacitance of an inverter that can deliver the same output current.
10	**Define path logical effort.** The logical effort along a path compounds by multiplying the logical efforts of all the logic gates along the path.
11	**What are the sources of power dissipation?** • Static power dissipation (due to leakage current when the circuit is idle) • Dynamic power dissipation (when the circuit is switching) and Short-circuit power dissipation during switching of transistors.
12	**What is static power dissipation?** Power dissipation due to leakage current when the circuit is idle is called the static power dissipation. Static power due to • Sub-threshold conduction through OFF transistors. • Tunneling current through gate oxide. • Leakage through reverse biased diodes. Contention current in ratioed circuits.
13	**What are the methods to reduce dynamic power dissipation?** • Reducing the product of capacitance and its switching frequency. • Eliminate logic switching that is not necessary for computation. • Reduce activity factor. Reduce supply voltage.
14	**What are the characteristics of CVSL?** • CVSL is a differential type of logic circuit whereby both true and complement inputs are required. • N pull down trees are the dual of each other. • P pull up devices are cross coupled to latch output. Both true and complement outputs are obtained.
15	**What is dynamic CMOS logic?** • Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes. Requires only N+2 transistors.
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17	**What are glitches?** A node exhibiting multiple transitions in a single clock cycle before settling to the correct logic level is called glitches or dynamic hazards. The occurrence of glitching in a circuit is mainly due to mismatch in the path lengths in the network.
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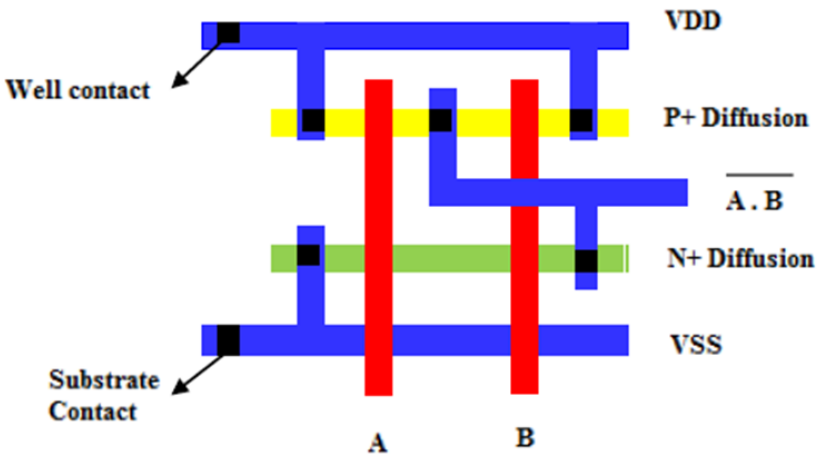
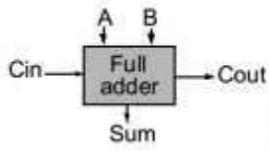
19	**Sketch the layout of a 2-input NAND gate.** 
20	**List out the sources of static and dynamic power consumption.** CMOS devices have very low static power consumption, which is the result of leakage current. But, when switching at a high frequency, dynamic power consumption can contribute significantly to overall power consumption. Charging and discharging a capacitive output load further increases this dynamic power consumption.
	UNIT III(2 marks)
1	**Define combinational and sequential circuit.** A combinational circuit consists of logic gates whose outputs at any time are determined from the present combination of inputs. On the other hand a sequential circuit in which the output depends on previous as well as current inputs. They can be used to keep a record of what value a variable (input, output or intermediate) had in the past as well as store the current value of a variable for later use.
2	**What is sequencing element?** Sequential circuits are designed with flip flops or latches, which are sometimes called memory elements that hold data called tokens. They can be used to keep record of what value (previous token) a variable had in the past as well as store the current (current token) value of a variable. They are used to _sequence‘ data, i.e. make a large amount of data appear in a pre-determined bit by bit sequence, they are called as sequencing elements.
3	**What is sequencing overload?** Sequencing elements delay tokens that arrive too early, preventing them from catching up with the previous tokens. Unfortunately, they inevitably add some delay to tokens that are already critical, decreasing the performance of the system. This extra delay is called sequencing overload.
4	**Define metastability.** Flip flop is a device that is susceptible to metastability. It has two well defined stable states, traditionally designated 0 and 1, but under certain conditions it can hover between them for longer than a clock cycle. This condition is known as metastability. Such a metastable –state is considered a failure mode of the logic design and timing constraints. The most common cause of metastability is violating the flip-flop‘s setup and hold times. During the time from the setup to the hold time, the input of the flip-flop should remain in a stable logic state; a change in the input in that time will have a probability of setting the flip-flop to a metastable state.

5	**Define metastable condition.** In reality, when a flip flop samples as input that is changing during its aperture, the output Q may momentarily take on a voltage between 0 and VDD that is in the forbidden zone. This is called a metastable state. Eventually, the flip flop will resolve the output to a stable state of either 0 or 1.
6	**Define logic propagation delay (t_{pd}).** Upper bound on interval between valid inputs and valid outputs.
7	**Define logic contamination delay (t_{cd}).** Lower bound on interval between invalid inputs and invalid outputs.
8	**List the methods of sequencing static circuits.** The three most widely used methods of sequencing static circuits • Flip flops • 2-Phase transparent latches • Pulsed latches
9	**Define min-delay failure.** In a sequential circuit if the hold time is large and the contamination delay is small, data can incorrectly propagate through two successive elements on one clock edge, corrupting the state of the system. This is called a race condition, hold time failure or min-delay failure.
10	**Define time borrowing.** The principle advantage of transparent latches over flip flops is the softer edges that allow data to propagate through the latch as soon as it arrives instead of waiting for a clock edge. Therefore, logic does not have to be divided exactly into half cycles. Some logic blocks can be longer while others are shorter, and the latch based system will tend to operate the average of the delays; a flip flop based system would operate at the longest delay. This ability of slow logic in one half-cycle to use timenormally allocated to faster logic in another half-cycle is called time borrowing or cycle stealing.
11	**What is clock skew?** In reality clocks have some uncertainty in their arrival times that can cut into the time available for useful computation is called clock skew.
12	**What are the different types of pipelines?** Depending on the data forwarded fashion namely, when applied to new data, pipelining techniques can be classified into synchronous pipelining, asynchronous pipelining and wave pipelining. In the synchronous pipelining, new data are applied to a computational circuit in intervals determined by the maximum propagation delay of the computational circuit. In the asynchronous pipelining, new data are applied to a computational circuit in intervals determined by the average propagation delay of the computational circuit. In the wave pipelining, new data can be applied to a computational circuit in intervals determined by the difference between maximum and minimum propagation delays of the computational circuit.
13	**What are the approaches used in the design of asynchronous pipeline systems?** An asynchronous design is based on the concept of modular functional blocks intercommunicating using some communication protocols. The general approaches of asynchronous pipeline systems are one way control and two way control. The one way control is also called a strobe control and the two way control scheme is generally referred to as a handshaking control.
14	**What is resettable latch?**

	Resettable latches and flip-flops employs a control input called reset signal to enter a known initial state on startup.
15	**What are the two types of reset?** The two types of reset are (i) Synchronous (ii) Asynchronous In synchronous reset, the flip-flop changes with synchronous control inputs and clock signal. In asynchronous reset, the output is independent of the synchronous input and the clock input.
16	**What is differential flip-flop?** Differential flip-flops accept true and complementary inputs and produce true and complementary outputs. This can be built from a clocked sense amplifier so they can rapidly respond to small differential input voltages.
17	**What is synchronizers?** A synchronizer is a circuit that accepts an input that can change at arbitrary times and produces an output aligned to the synchronizer‘s clock. Because the input can change during the synchronizer‘s aperture, the synchronizer has a non zero probability of producing a metastable output.
18	**What is arbiter?** An arbiter is a circuit designed to determine which of several signals arrive first. Arbiters are used in asynchronous circuits to order computational activities for shared resources to prevent concurrent incorrect operations.
19	**What is mesochronous interconnect?** A mesochronous signal is one that has the exactly same frequency as a local clock, and maintains unknown phase offset to that clock.
20	**What is plesiochronous interconnect?** A plesiochronous signal is one that has almost the same frequency as a local clock, resulting in slowly drifting phase offset to that clock.
	UNIT IV(2 marks)
1	**What is datapath?** A datapath is the data processing section of a processor. It consists of several multiple-bit data path elements or operators such as arithmetic units (adder, multiplier, shifter, comparator) or logical operators (AND, OR, NAND) arranged horizontally and connected with buses. Control signals connect to the datapath at the top and bottom.
2	**What is bit slice operation?** Bit slicing is a technique for constructing a particular word length of block from modules of smaller bit width. Each of these components processes one bit field or –slice of an operand. The grouped processing components would then have the capability to process the chosen full word-length.
3	**What are the disadvantages of full adder design using static CMOS?** The major shortfalls associated with the static CMOS full adder are: • Large PMOS transistor in pull up network result in high input capacitances, which cause high delay and dynamic power. • The critical path delay of SUM sub-circuit depends on the signal statistics of CARRY sub- block and inverter delay. Therefore the propagation delay is high in the static CMOS full adder realization. • The intrinsic load capacitance of the CARRY signal is high which is contributed by the gates capacitances C1, C2, C3, C4, C5 and C6, diffusion capacitances in stage 1 and stage 2 and wiring capacitance. • This adder realization consumes a large area and it could possible to fabricate

in twin-tub CMOS process to avoid mobility degradation and latch up condition.

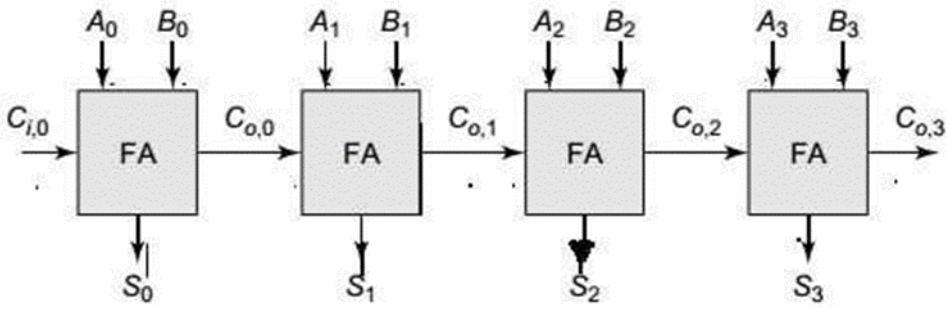
4 **Draw the truth table of a binary full adder and write the expressions for sum and carry output.**



A	B	C_i	S	C_o	*Carry status*
0	0	0	0	0	delete
0	0	1	1	0	delete
0	1	0	1	0	propagate
0	1	1	0	1	propagate
1	0	0	1	0	propagate
1	0	1	0	1	propagate
1	1	0	0	1	generate
1	1	1	1	1	generate

$$S = A \oplus B \oplus C_i$$
$$= A\bar{B}\bar{C}_i + \bar{A}B\bar{C}_i + \bar{A}\bar{B}C_i + ABC_i$$
$$C_o = AB + BC_i + AC_i$$

5 **Draw the topology of a four bit ripple carry adder.**



6 **What are the main stages of an array multiplier?**
The main stages of an array multiplier are: partial product generation, partial product accumulation and final addition.

7 **What are the main stages of an array multiplier?**
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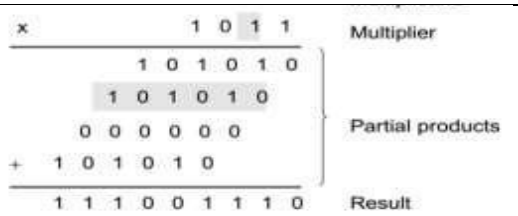
8 **Illustrate binary multiplication using a simple example. Specify the bit size of the inputs and the partial products.**

	
9	**What is the necessity of a level converter? Draw a simple circuit of the same.** When combining multiple supply voltages on a die, level converters are required whenever module at the lower power supply has to drive a gate at the higher voltage. If a gate supplied by VDDL drives agate at VDDH, the PMOS transistor never turns off, resulting in static current and reduced output swing. A level conversion performed at the boundaries of supply voltage domains prevents these problems.
10	**What method is adopted to reduce power in idle mode?** A common method to reduce power in idle mode is clock gating. In this method, the main clock connection to a module is turned off (or gated) whenever the block is idle. However clock gating
11	**List the different considerations for designing a Ripple carry adder.** • Propogation delay of ripple carry adder is linearly proportional to N. • It is important to optimize tcarry than tsum. Inverting all i/ps to a full adder results in inverted values for all o/ps.
12	**What are the draw backs of a static adder circuit?** • Consumes large area. Circuit is slow.
13	**What is the advantage of Dynamic Supply Voltage Scaling (DVS)?** Lowering the clock frequency when executing the reduced workloads reduces the power but does not save energy- every operation is still executed at the high voltage level. However if both supply voltage and frequency are reduced simultaneously, the energy is reduced. In order to maintain the required throughput for high workloads and minimize energy for low workloads, both supply and frequency must be dynamically varied according to the requirements application that is currently being executed. This technique is called Dynamic Supply Voltage Scaling (DVS).
14	**What are the parts of a DVS system?** A practical implementation of the DVS system consists of the following: • A processor that operate at a wide variety of supply voltages. • A power regulation loop that sets the minimum voltage necessary for operation at a desired • frequency An operating system that calculates the desired frequencies to meet required throughputs and task completion deadlines.
15	**Illustrate threshold voltage control in an inverter.** Substrate bias is the control knob that allows us to vary the threshold voltages dynamically. In order to do so, we have to operate the transistors as four- terminal devices. Variable threshold voltage scheme can accomplish a variety of goals: • It can lower the leakage in standby mode • It can compensate for threshold voltage variations across the chip during normal operation of the circuit • It can throttle the throughput of the circuit to lower both the active and leakage

	power based on performance requirements
16	**Why is static adder circuit slow?** static adder ckt is slow as, • Long chains of series PMOS transistors are present in both carry & Sum generation circuit. • Intrinsic load capacitance of the Co signal is large & consists of 2 diffusion & 6 gate capacitances plus the wiring g capacitances. • Carry generation ckt requires 2 inverting stages per bit. Sum generation ckt requires an extra logic stage
17	**What is the advantage of Dynamic adder design?** Reduced capacitance of dynamic circuitry results in substantial speed up over static implementation.
18	**Write the principle of any one fast multiplier?** Booth multiplier is a radix -4 multiplication scheme , which examines 3 bits of the multiplicand at a time to determine whether to add 0,1,-1,2,-2 of that rank of the multiplicand.
19	**Define throughput.** A metric called throughput is often used as a measure of the utilization of a microprocessor system. The throughput is the number of operations for the number of instructions performed over a unit period of time. The throughput is typically described in terms of either millions of operations per second or million of instructions per second.
20	**Give the application of high speed adder.** High speed Adders will reduce the hardware complexity and make justice with Speed Power,Area and Accuracy metrics. Adders are one of the key components in arithmetic circuits. Approximation can increase performance or reduce power consumption with a simplified or inaccurate circuit in application contexts where strict requirements are relaxed. The potential application is in the DSP application for portable devices such as cell phones and laptops.
	UNIT V(2 marks)
1	**What is an FPGA?** FPGA is Field Programmable Gate Array that consists of an array of anywhere from 64 to 1000s of logic gate groups that are sometimes called configurable logic blocks.
2	**What is SOG?** A channelless gate-array is called sea-of-gates (SOG) array. The core area of the die is completely filled with an array of base cells (the base array).
3	**Compare FPGA and CPLD?** **CPLD's** have a much higher capacity than simple PLDs, permitting more complex logic circuits to be programmed into them. A typical CPLD is equivalent of from 2 to 64 simple PLDs. The development of these devices followed simple PLD as advances in technology permitted higher density chips to be implemented. There are several forms of CPLD, which vary in complexity and programming capability. CPLDs typically come in 44 to 160 pin packages depending on the complexity. **FPGA** are different from simple PLDs and CPLDs in their internal organization and have the greatest logic capacity. FPGAs are consists of an array of anywhere from 64 to 1000s of logic gate groups that are sometimes called logic blocks. Two basic classes

of FPGAs are fine grained and course grained .The course grained FPGA has large logic blocks and fine grained FPGAs has much
smaller logic blocks. FPGAs are come in packages up to 1000 pins or more.

4 **Differentiate CBIC & Gate array logic?**

CBIC	Gate array logic
Cell-based IC uses predesigned logic cells (AND gates, OR gates, multiplexers, and flip-flops, for example)	In a gate array (GA) or gate-array–based ASIC the transistors are predefined on the silicon wafer.
CBIC means a standard-cell–based ASIC	it is often called a masked gate array (MGA).
The standard-cell areas in a CBIC are built of rows of standard cells. The standard-cell areas may be used in combination with larger predesigned cells, known as megacells.	The logic cells in a gate-array library are often called macros.

5 **List out three main parts of FPGA & what is PMS?**

- CLB-Configurable Logic Block
- IOB-Input Output Block

PMS-Programmable Switch Matrix

6 **List the types of ASIC?/ State the different types of ASICs.**

- Full-Custom ASICs
- Semicustom ASICs :

– Standard-Cell–Based ASICs

7 **What is Full custom ASIC?/What are the features of full custom ASIC?**

To modify according to a customer's individual requirements, All mask layers are customized in a full custom ASIC

- Generally, the designer lays out all cells by hand
- Some automatic placement and routing may be done
- Critical (timing) paths are usually laid out completely by hand

Full-custom design offers the highest performance and lowest part cost (smallest die size) for a given design. The manufacturing lead time (the time it takes just to make an IC—not including design time) is typically eight weeks for a full-custom IC.

8 **Write the objectives and Goals of System Partitioning.**

The goal of partitioning is to divide this part of the system so that each partition is a single ASIC. To do this we may need to take into account any or all of the following objectives:

- A maximum size for each ASIC
- A maximum number of ASICs
- A maximum number of connections for each ASIC

A maximum number of total connections between all ASICs

9 **What is fully PCI in Spartan-II FPGA?**

Fully Peripheral Component Interface (PCI) used to interface components.

10 **Differentiate fine-grain and coarse-grain architecture of FPGA** BTL4

tasks without wasting reconfigurable resources	Reconfigurable resources are wasted during data manipulation
For large and complex calculations numerous fine-grained PEs are required to implement a basic computation	Fewer coarse-grained PEs are required to implement a basic computation
Much slower clock rates	Faster
Extremely costly relative to coarse-grained architectures	Less Expensive
Supports partial array configuration and is dynamically reconfigurable during application execution.	Both partially and dynamically reconfigurable

11 **State the Xilinx FPGA design flow.**

- Specification
- VHDL description - Functional simulation
- Synthesis - Post-synthesis simulation
- Implementation - Timing simulation

Configuration - On chip testing

12 **What are the different types of interconnections present in Xilinx FPGA?**

Direct interconnect: Adjacent CLBs are wired together in the horizontal or vertical direction. The most efficient interconnect.

General-purpose interconnect: used mainly for longer connections or for signals with a moderate fanout.

Long line interconnect: for time critical signals (e.g. clock signal need be distributed to many CLBs)

13 **What is meant by speed grading?**

Most of the FPGA header short chip according to speed is called speed binning or speed grading. According to Xilinx FPGA product, The speed grade specify the transistor switching speed that determines how quickly internal clocked circuits can be activated.

14 **What is meant by BIDA?**

The Bidirectional Interconnect Buffers (BIDA) restore the logic level and logic strength on long interconnect paths.

15 **List the advantages of Global routing.**

We typically global route the whole chip (or large pieces if it is a large chip) before detail routing the whole chip (or the pieces). There are two types of areas to global route: inside the flexible blocks and between blocks.

The goal of global routing is to provide complete instructions to the detailed router on where to route every net. The objectives of global routing are one or more of the following:

- Minimize the total interconnect length.
- Maximize the probability that the detailed router can complete the routing.

Minimize the critical path delay.

16 **What are feedthrough cells? State their uses.**

The term feedthrough cells can refer either to a piece of metal that is used to pass a signal through a cell or to a space in a cell, waiting to be used as a feed through.

17 **What is the standard cell-based ASIC design?**

In cell based design, the designer reuses the cells that have already been designed and stored in the library as a part of the current design. Cell – based IC used predesigned

	logic cells(AND gates, OR gates, multiplexers and flip flop). CBIC means standard cell based ASIC. The standard-cell areas in a CBIC are built of rows of standard cells. The standard-cell areas may be used in combination with larger predesigned cells known as mega cells.
18	**Name the elements in a Configurable Logic Block** Flip flops to store data and Look up tables and Multiplexers to implement logic.
19	**What is meant by CBIC?** Cell – based IC used predesigned logic cells (AND gates, OR gates, multiplexers and flipflop). CBIC means standard cell based ASIC. The standard-cell areas in a CBIC are built of rows of standard cells. The standard-cell areas may be used in combination with larger predesigned cells known as megacells.
20	**What is an antifuse? State its merits and demerits.** An antifuse is an electrical device that performs the opposite function to a fuse. Whereas a fuse starts with a low resistance and is designed to permanently break an electrically conductive path (typically when the current through the path exceeds a specified limit), an antifuse starts with a high resistance and is designed to permanently create an electrically conductive path (typically when the voltage across the antifuse exceeds a certain level). **Demerits:** The size of an antifuse is limited by the resolution of the lithography equipment used to makes ICs. The Actel antifuse connects diffusion and polysilicon, and both these materials are too resistive for use as signal interconnects. To connect the antifuse to the metal layers requires contacts that take up more space than the antifuse itself, reducing the advantage of the small antifuse size. However, the antifuse is so small that it is normally the contact and metal spacing design rules that limit how closely the antifuses may be packed rather than the size of the antifuse itself. **Merits:** There are two advantages of a metal–metal antifuse over a poly–diffusion antifuse. The first is that connections to a metal–metal antifuse are direct to metal—the wiring layers. Connections from a poly–diffusion antifuse to the wiring layers require extra space and create additional parasitic capacitance. The second advantage is that the direct connection to the low- resistance metal layers makes it easier to use larger programming currents to reduce the antifuse resistance. Average QuickLogic metal–metal antifuse resistance is approximately 80 W (with a standard deviation of about 10 W) using a programming current of 15 mA as opposed to an average antifuse resistance of 500 W (with a programming current of 5 mA) for a poly–diffusion antifuse.