SUBJECT NAME : DIGITAL SYSTEMS DESIGN
SUBJECT CODE : EC3352

IMPORTANT QUESTIONS

PART – A

UNIT - I

DIGITAL FUNDAMENTALS

1. **State Demorgan's Theorem.**

   De Morgan suggested two theorems that form important part of Boolean algebra. They are,

   i. The complement of a product is equal to the sum of the complements.

   $(AB)' = A' + B'$

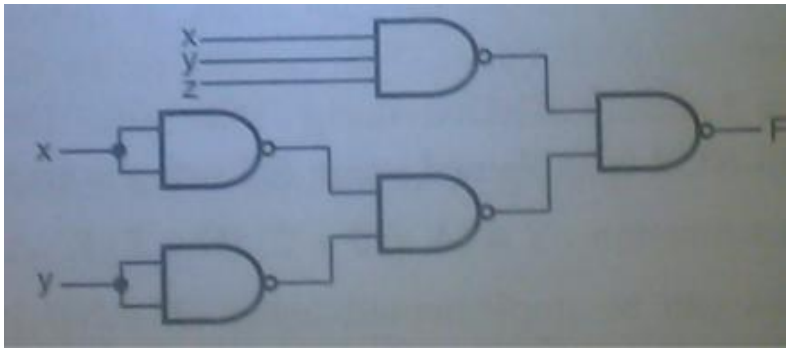
A	B	$\overline{AB}$	$\overline{A}+\overline{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

   ii. The complement of a sum term is equal to the product of the complements.

   $(A + B)' = A'B'$

A	B	$\overline{A+B}$	$\overline{A}\,\overline{B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

2. **Implement using NAND gates only, *F = x y z + x′ y′.***



3. What are Don't care terms?

In some logic circuits certain input conditions never occur, therefore the corresponding output never appears. In such cases the output level is not defined, it can be either high or low. These output levels are indicated by 'X' or 'd' in the truth tables and are called don't care conditions or incompletely specified functions.

4. Apply De-Morgan's theorem to *[(A+B) + C] '.*

Given $[(A+B)+C]' = (A+B)'.C'$

$= (A'.B').C'$

$$[(A+B)+C]' = A'B'C'$$

5. Convert 0.35 to equivalent hexadecimal number.

Given $(0.35)_{10}$ =0.35 x 16=5.60
=0.60 x 16=9.60
=0.60 x 16=9.60

$$(0.35)_{10} = (0.599)_{16}$$

6. Convert *Y=A+BC'+AB+A'BC* into canonical form.

Given $Y=A+BC'+AB+A'BC$

$Y=A(B+B')(C+C')+(A+A')BC'+AB(C+C')+A'BC$

$Y=ABC+ABC'+AB'C+AB'C'+ABC'+A'BC'+ABC+ABC'+A'BC$

$$Y=ABC+ABC'+AB'C+AB'C'+A'BC'+A'BC$$

7. Define 'min term' and 'max term'.

A product term containing all the variables of the function in either complemented or uncomplemented form is called a min term.

A sum term containing all the variables of the function in either complemented or uncomplemented form is called a max term.

8. Prove that the logical sum of all min terms of a Boolean function of 2 variables is 1.

Consider two variables as A and B. For two variables A and B minterms are:
A′B′,A′B,AB′,AB. The logical sum of these minterms are given by
F= A′B′+A′B+AB′+AB

= A′(B′+B)+A(B′+B) (B′+B=1)
= A′(1)+A(1) (A′+A=1)

F=1
Hence it is to be proved.

9. Show that a positive logic NAND gate is a negative logic NOR gate.

Truth Table for NAND Gate		
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

≡

Truth Table for Positive Logic NAND Gate		
A	B	Y
LOW	LOW	HIGH
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	LOW

Truth Table for NOR Gate		
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

≡

Truth Table for Negtive Logic NOR Gate		
A	B	Y
HIGH	HIGH	LOW
HIGH	LOW	HIGH
LOW	HIGH	HIGH
LOW	LOW	HIGH

Truth table for positive logic NAND gate and negative logic NOR gates are same and hence a positive logic NAND gate is negative logic NOR gate.

10. Simplify the following Boolean Expression to a minimum number of literals.

(BC'+A'D)(AB'+CD')

F=(BC′+A′D)(AB′+CD′)

=BC′AB′+BC′CD′+A′DAB′+A′DCD′ (A.A′=0)

= AB B′C′+BCC′D′+AA′ B′D+A′CDD′

F=0

11. Simplify the given Boolean Expression *F=x′+xy+xz′+xy′z′.*

F=x′+xy+xz′+xy′z′

= x′+x(y+z′+y′z′) (A+A′B=A+B)

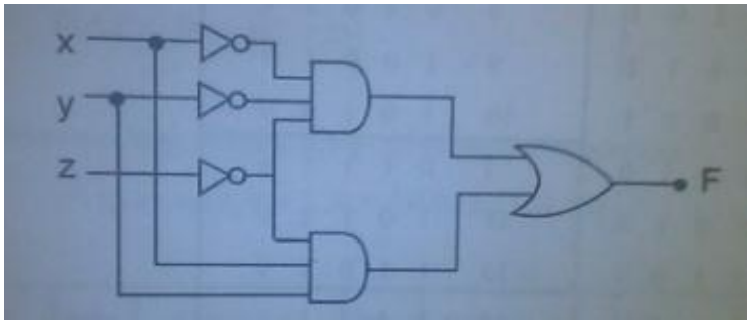
= x′+y+z′+y′z′

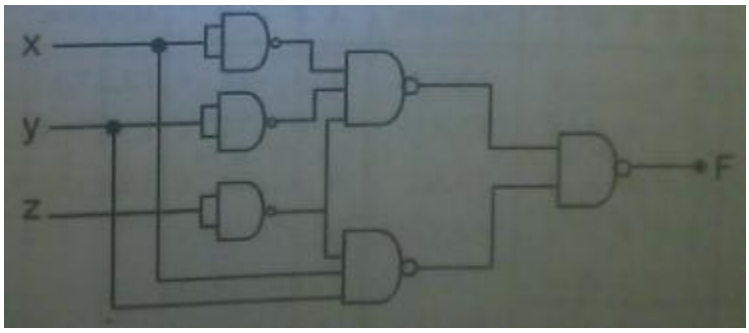
= x′+y+z′(1+y′) (1+A′=1)

F = x′+y+z′

12. Implement the given function using NAND gates *F(x,y,z)= Σm(0,6).*

F(x,y,z)=x'y'z'+xyz'





13. State Distributive Law.

Distributive law of dot(.) over plus(+) is given by **a.(b+c) = a.b + a.c**

Distributive law of plus(+) over dot(.) is given by **a+b.c = (a+b).(a+c)**

14. What is Prime Implicant?

A prime implicant is a group of minterms which cannot be combined with any other minterms or groups.

15. Simplify the following Boolean expression into one literal.
W'X(Z'+YZ)+X(W+ Y'Z)

F= *W'X(Z'+YZ)+X(W+ Y'Z)*

= *W'XZ'+W'XYZ+WX+XY'Z*
=*X(W'Z'+W'YZ+W+Y'Z)*

= *X(W'Z'+W+Z(Y'+W'Y))*
= *X(W'Z'+W+Z(Y'+ Y)(Y'+W'))*

= *X(W'Z'+W+Z(Y'+W'))*
= *X(W'Z'+W+ZY'+W'Z)*

= ***X(W'(Z'+Z)+W+ZY')***
= *X(1+W+ZY')*
= *X(1+ZY')=X.1*

F =X

UNIT - 2

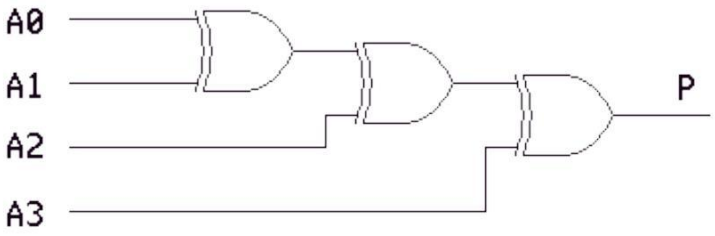
COMBINATIONAL CIRCUIT DESIGN

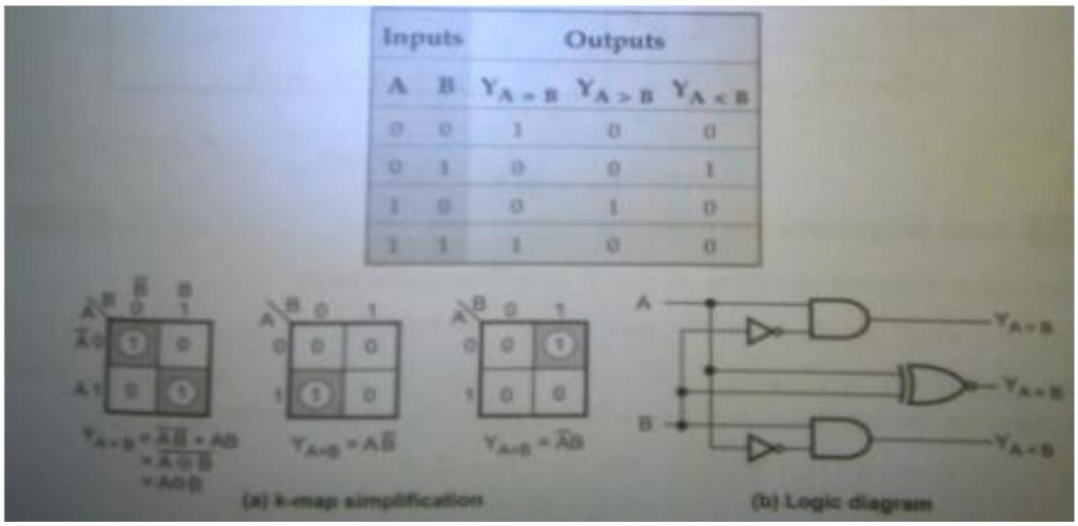
1 Write an expression for borrow and difference in a full subtractor circuit.

Difference = $A'B+AB'=A \oplus B$

Borrow = $A'B$

2 Design a single bit magnitude comparator to compare two words A and B.





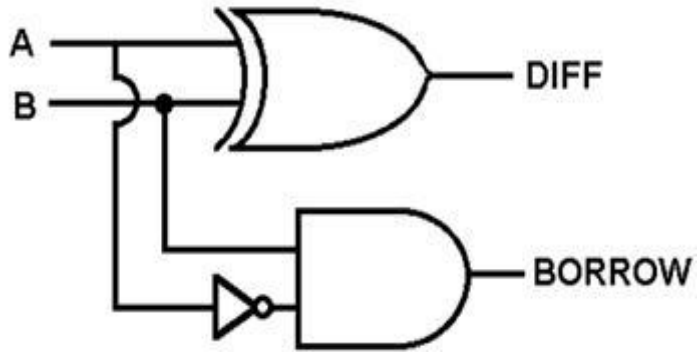
3 What is an encoder?

An encoder has 2^n input lines and n output lines. In encoder the output lines generate the binary code corresponding to the input value.

4 List few applications of multiplexer.

- Data Selector.
- Implement combinational logic circuit.
- Time multiplexing systems
- Frequency multiplexing systems.
- D/A and A/D converter
- Data acquisition systems.

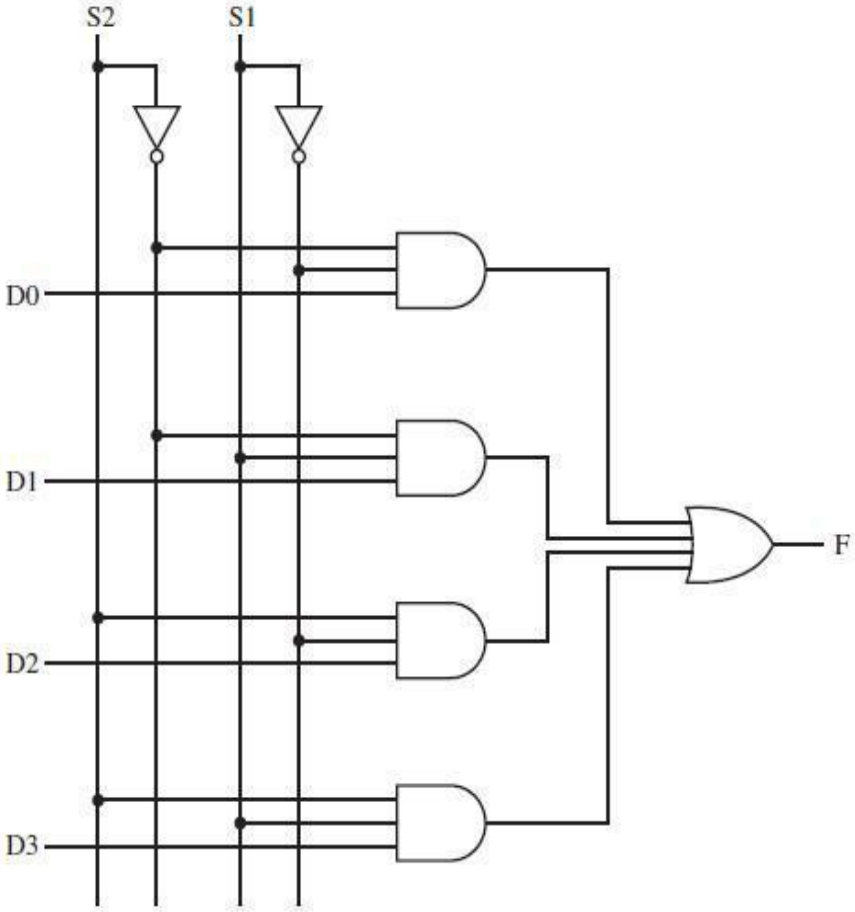
5 Design a half subtractor using basic gates.



Difference=A′B+AB′=A⊕B

Borrow=A′B

6 Draw the logic diagram of a 4 line to 1 line multiplexer.



7. What is priority Encoder?

A priority encoder is an encoder circuit that includes the priority function. In priority encoder, if 2 or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

8. Write down the difference between demultiplexer and decoder.

	Demultiplexer	Decoder
Definition	1 data input 2^n outputs	It has n inputs 2^n outputs It has n control inputs
Characteristic	Connects the data input to the data output	Selects one of the 2^n outputs by decoding the binary value on the basis of n inputs
Reverse of	Multiplexer	Encoder

9 Give the logic expression for sum and carry in full adder circuit.

SUM = $(A \oplus B) \oplus C_{IN}$

CARRY = $AB+BC_{IN}+A\ C_{IN}$

10 Give examples for combinational circuit.

i. Adders

ii. Subtractors

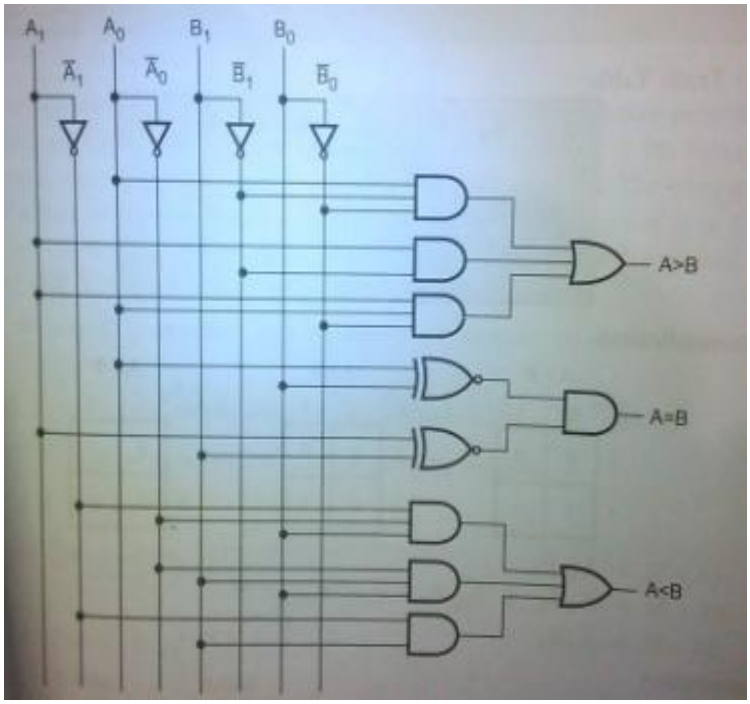
iii. Multiplexers

iv. Demultiplexers

v. Encoders

vi. Decoders

11 Draw the logic circuit of a 2-bit comparator.[April/May-2015,2014]



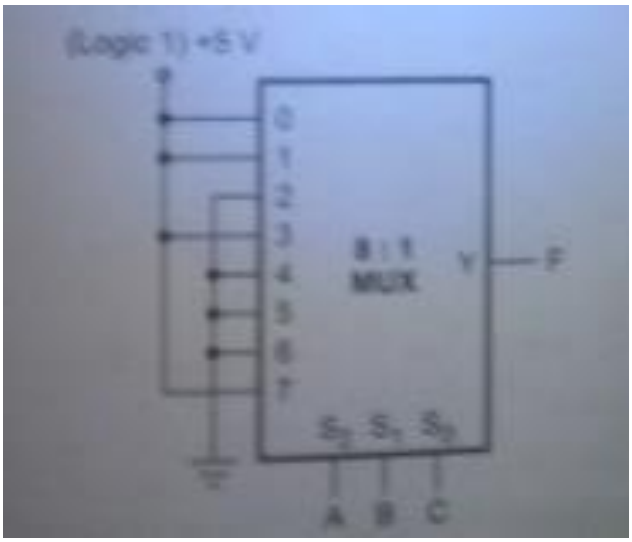
12 Suggest a solution to overcome the limitation on the speed of an adder.

It is possible to increase speed of adder by eliminating inter-stage carry delay. This method utilizes logic gates to look at the lower-order bits of the augend and addend to see if a higher-order carry is to be generated.

13 Relate carry generate, Carry propagate, Sum and Carry-out of a Carry look a head adder.

$$P_i = A_i \oplus B_i$$
$$G_i = A_i \cdot B_i$$
$$C_{i+1} = G_i + (P_i \cdot C_i)$$
$$C_1 = G_0 + P_0 \cdot C_0$$
$$C_2 = G_1 + G_0 \cdot P_1 + C_0 \cdot P_0 \cdot P_1$$
$$C_3 = G_2 + G_1 \cdot P_2 + G_0 \cdot P_1 \cdot P_2 + C_0 \cdot P_0 \cdot P_1 \cdot P_2$$
$$C_4 = G_3 + G_2 \cdot P_3 + G_1 \cdot P_2 \cdot P_3 + G_0 \cdot P_1 \cdot P_2 \cdot P_3 + C_0 \cdot P_0 \cdot P_1 \cdot P_2 \cdot P_3$$

14. Realize the Boolean function using appropriate multiplexer *F(A,B,C)= Σ (0,1,3,7)*



15. Compare the performance of binary serial and parallel adders.

Serial Adder:

- Serial adder uses shift registers
- The serial adder requires only one full adder circuit
- The serial adder is a sequential circuit
- Time required for addition depends on the number of bits

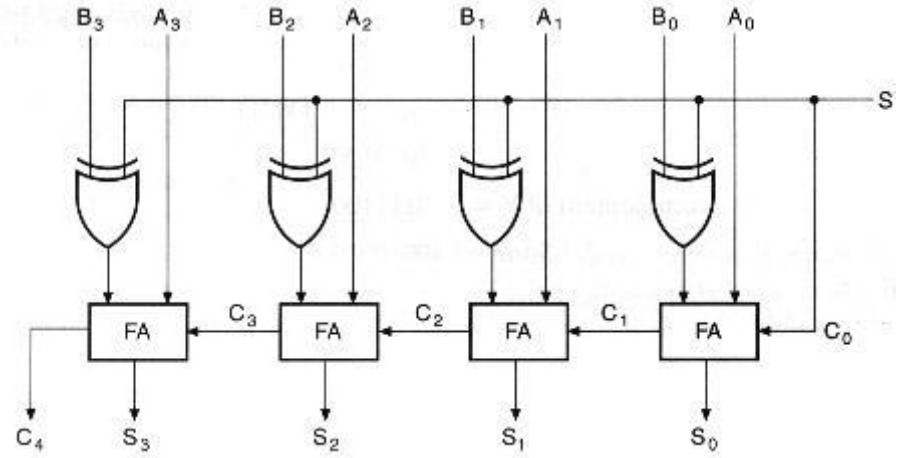
- It is slower

parallel adder:

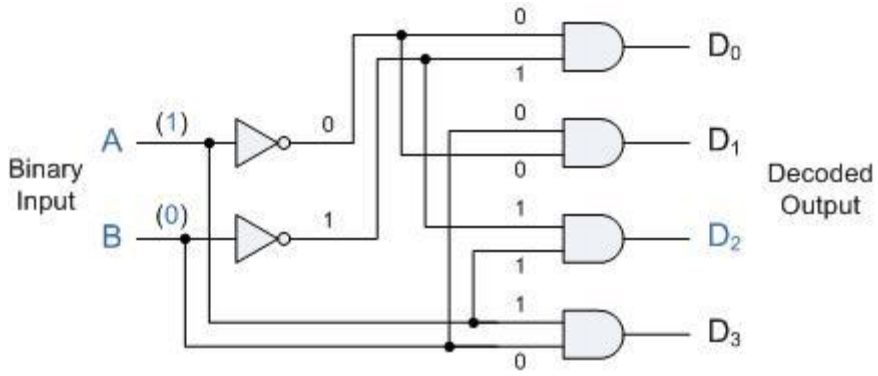
- Parallel adder uses registers with parallel load capacity

- It is faster
- Time required for addition does not depend on number of bits
- Excluding the registers, the parallel adder is a purely combinational circuit

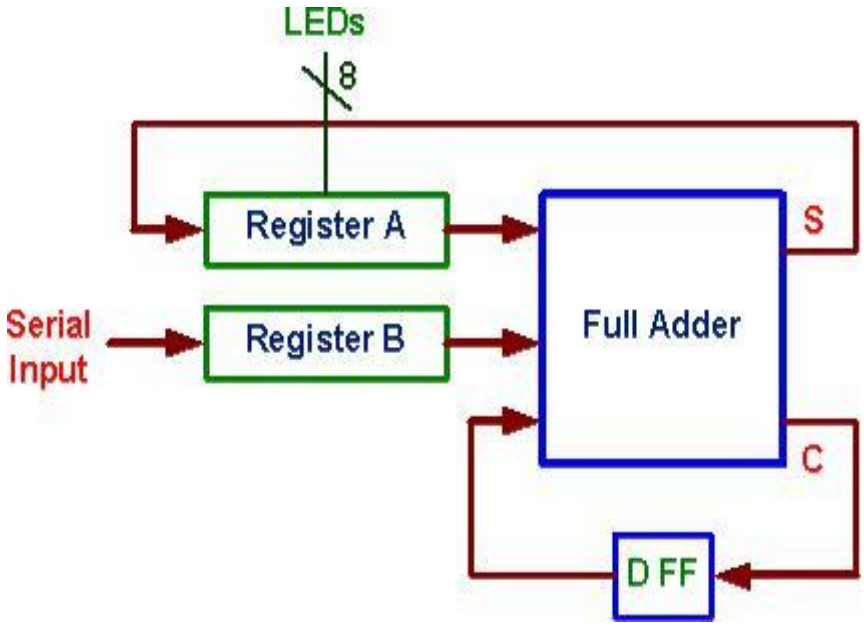
16. **Construct a two-4-bit parallel adder/subtractor using Full Adders and XOR gates.**



17. **Convert a two-to-four line decoder with enable input to 1X4 Demultiplexer**



18. **Draw the logic diagram of serial adder.**



UNIT- 3

SYNCHRONOUS SEQUENTIAL CIRCUITS

1. **Mention any two differences between the edge triggering and level triggering.**

Level Triggering:

1) The input signal is sampled when the clock signal is either HIGH or LOW.

2) It is sensitive to Glitches.

Example: Latch.

Edge Triggering:

1) The input signal is sampled at the RISING EDGE or FALLING EDGE of the clock signal.

2) It is not-sensitive to Glitches.
Example: Flipflop.

2. **What is meant by programmable counter? Mention its application.**

- A counter that divides an input frequency by a number which can be programmed into decades of synchronous down counters.
- Decades, with additional decoding and control logic, give the equivalent of a divide-by *N* counter system, where *N* can be made equal to any number.

Application:

- Microprocessor.
- Traffic light controller.
- Street light controller.

3. **Write the characteristic equation of a JK flip-flop.**

The characteristic equation of a JK flip-flop is given by

$$Q(next) = JQ' + K'Q$$

4. State the differences between Moore and mealy state machine.

1)Mealy Machines tend to have less states

a) Different outputs on arcs (n^2) rather than states (n).

2) Moore Machines are safer to use

a) Outputs change at clock edge (always one cycle later).
b) In Mealy machines, input change can cause output change as soon as logic is done

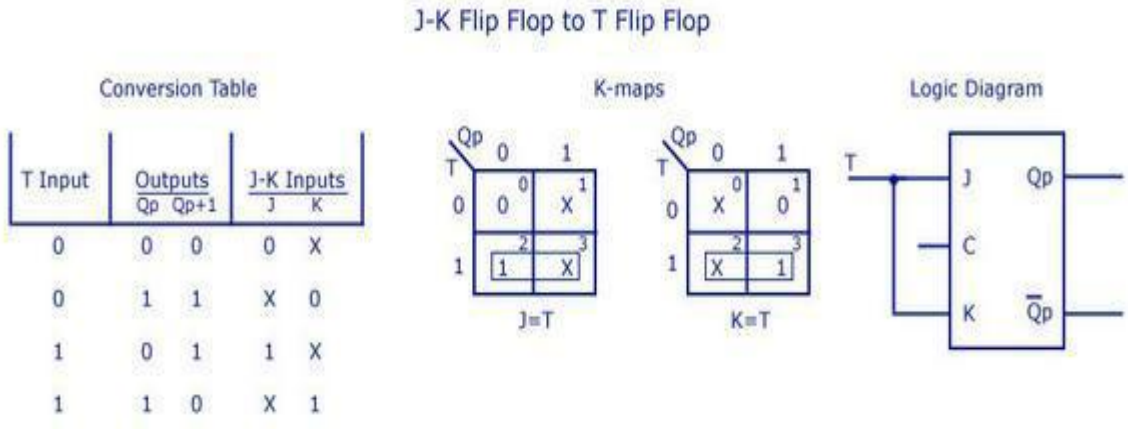
- A big problem when two machines are interconnected asynchronous feedback.

3) Mealy Machines react faster to inputs

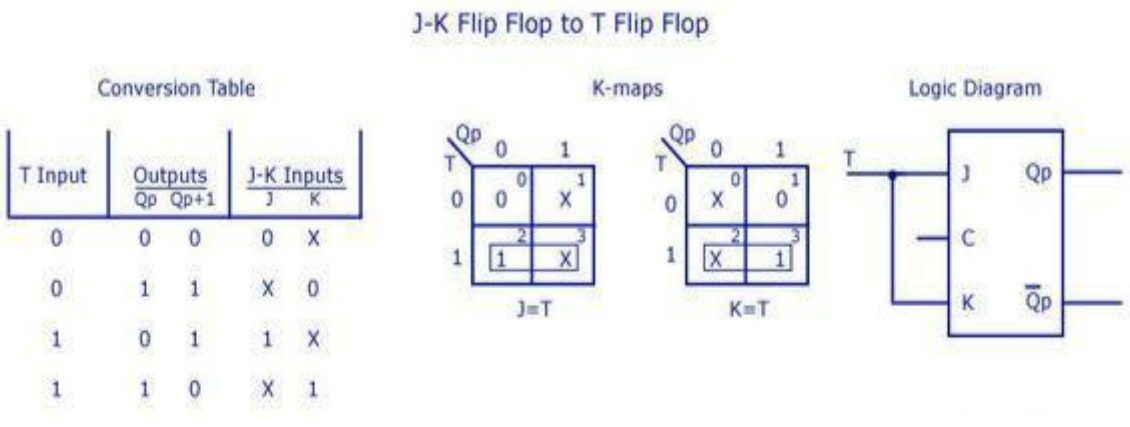
b) React in same cycle – don't need to wait for clock.

c) In Moore machines, more logic may be necessary to decode state into outputs – more gate delays after.

5. Realise T-FF from JK-FF.



6. Convert JK flip-flop to T flip-flop.



7. **How many flip-flops are required to build a binary counter that counts from 0 to 1023?**

   If the number of flip-flops required is n,
   then 2^n-1=1023 **n=10** since 2^{10}=1024

8. **Compare the logics of synchronous counter and ripple counter.**

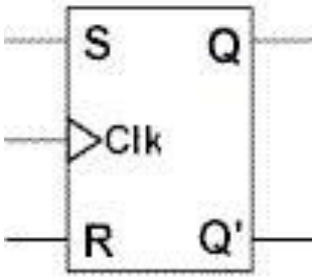
   Asynchronous counter:

   1. In this type of counter flipflop are connected in such a way that output of first flip-flop drives the clock for next flip-flop.
   2. All the flip-flop are not clocked simultaneously.
   3. Logic circuit is very simple even for more number of states.

   Synchronous counter:

   1. In this type there is no connection between output of first flip-flop and clock input of the next flip-flop.
   2. All the flip-flop are clocked simultaneously.
   3. Design involves complex logic circuit as number of states increases.

9. **Sketch the logic diagram of a clocked SR flip-flop.**



10. **How do you eliminate the race around condition in a JK flip-flop?**

- When the input to the JK flip-flop is j=1 and k=1, the race around condition occurs, i.e it occurs when the time period of the clock pulse is greater than the propagation delay of the flip flop.
- the output changes or toggles in a single clock period. If it toggles even number of times the output is same but if it toggles odd number of times then the output is complimented.

  To avoid race around condition we cant make the clock pulse smaller than the propagation delay so we use

  1. Master slave JK flip flop
  2. Positive or negative edge triggering

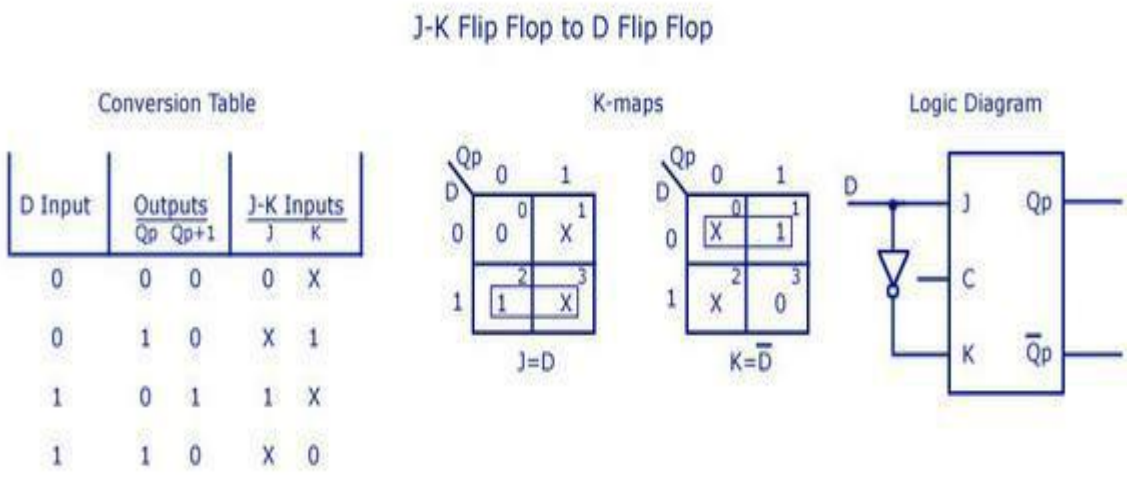
11. Draw the state table and excitation table of T flip-flop.

Q[t]	T	Q[T+1]	J	K
0	0	0	0	X
0	1	1	1	X
1	0	1	X	0
1	1	0	X	1

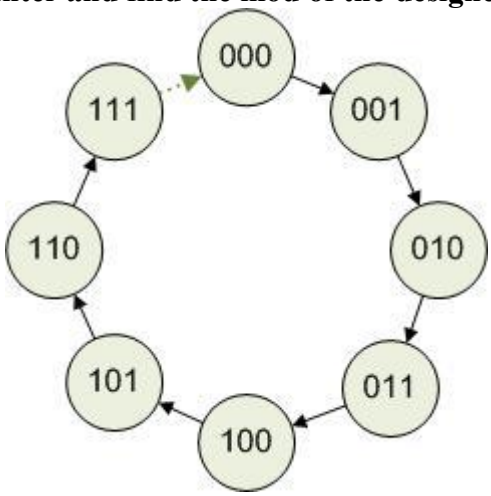
12. A 4-bit binary ripple counter is operated with clock frequency of 1KHz. What is the output frequency of its third Flip flop?

The output frequency of third flip-flop is: $½^3$ = **1/8KHz.**

13. Realize JK flip-flop using D flip-flop.



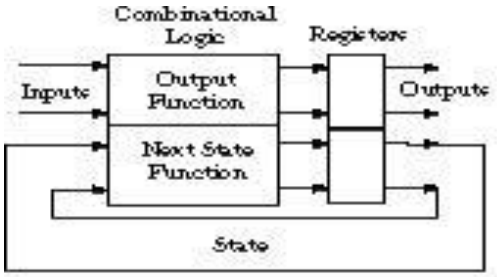
14. Design a 3-bit ring counter and find the mod of the designed counter.

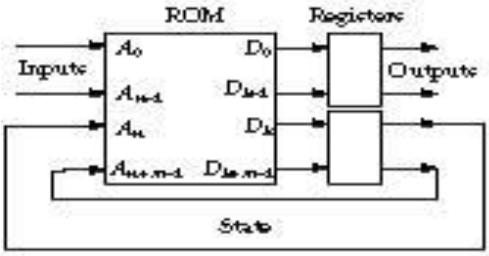


15. Define latches.

Latch is a simple memory element, which consists of a pair of logic gates with their inputs and outputs inter connected in a feedback arrangement, which permits a single bit to be stored.

16. Draw the block diagram for Moore model.





ROM implementation of a synchronous Mealy finite state machine.

17. What is synchronous sequential circuit?

- In synchronous circuits the input are pulses (or levels and pulses) with certain restrictions on pulse width and circuit propagation delay. Therefore synchronous circuits can be divided into ***clocked*** sequential circuits and ***uncklocked or pulsed*** sequential circuits.

- In a ***clocked*** sequential circuit which has flip-flops or, in some instances, gated latches, for its memory elements there is a (synchronizing) periodic clock connected to the clock inputs of all the memory elements of the circuit, to synchronize all internal changes of state

UNIT- 4

ASYNCHRONOUS SEQUENTIAL CIRCUITS

1. What are hazard free digital circuits?

A circuit which has no hazard like static-0-hazard and static-1-hazard is called hazard free digital circuit.

2. What are the two types of asynchronous sequential circuits?

- Fundamental mode circuit
- Pulse mode circuit

3. What is state table?

The state table representation of a sequential circuit consists of three sections labelled present state, next state and output. The present state designates the state of flip-flops before the occurrence of a clock pulse. The next state shows the states of flip-flops after the clock pulse, and the output section lists the value of the output variables during the present state.

4. What are Hazards?

The unwanted switching transients (glitches) that may appear at the output of a circuit are called Hazards.

5. What is a state diagram? Give an example.

A state diagram is a type of diagram used in computer science and related fields to describe the behaviour of systems. State diagrams require that the system described is composed of a finite number of states; sometimes, this is indeed the case, while at other times this is a reasonable abstraction. Many forms of state diagrams exist, which differ slightly and have different semantics.

6. Under what circumstances asynchronous circuits are prepared.

(i) Fundamental mode asynchronous circuits

(ii) Pulse mode asynchronous circuits

7. Differentiate fundamental mode and pulse mode asynchronous sequential circuits.

	Fundamental mode sequential circuits	Pulse mode sequential circuits.
1	(i) Memory elements are clocked flip-flops	(i) Memory elements are either unlocked flip - flops or time delay elements.
2	(ii) Easier to design	(ii) More difficult to design

8. Write short notes on Hazards.

The unwanted switching transients (glitches) that may appear at the output of a circuit are called Hazards.

- Static-0-Hazard
- Static-1-Hazard

UNIT - 5

MEMORY DEVICES AND DIGITAL INTEGRATED CIRCUITS

1. What is meant by memory Expansion? Mention its limit.

The memory expansion can be achieved in two ways: by expanding word size and expanding memory capacity.

Limitations:

1. Memory capacity upto 16Mbytes.
2. 24 address lines and 16 data lines.

2. What are the advantages of static RAM and Dynamic Ram?

Static RAM:

- Access time is less.
- Fast operation.

Dynamic Ram

- It consumes less power.
- Cost is low.

3. What is difference between PAL and PLA?

PLA:

Both AND and OR arrays are programmable and Complex
Costlier than PAL

PAL:

AND arrays are programmable OR arrays are fixed
Cheaper and Simpler

3. Implement the exclusive or function using ROM.

- Can implement multi-input/multi-output logic functions inside of ROM.
- Data outputs are the logic functions and the address lines are the logic function inputs.
- We create a ROM Table to store the logic functions.
- When an input (or address) is presented, the value stored in the specified memory location appears at the data outputs.
- Each data output represents the correct value for its logic function

4. **Compare Dynamic RAM with Static RAM.**

- Static Ram is very costly.
- Dynamic Ram is cheaper.
- Static Ram contains Transistors.
- Dynamic Ram contains Capacitors.
- Static Ram is used in L1 and L2 cache.
- Dynamic Ram is used in system RAM.

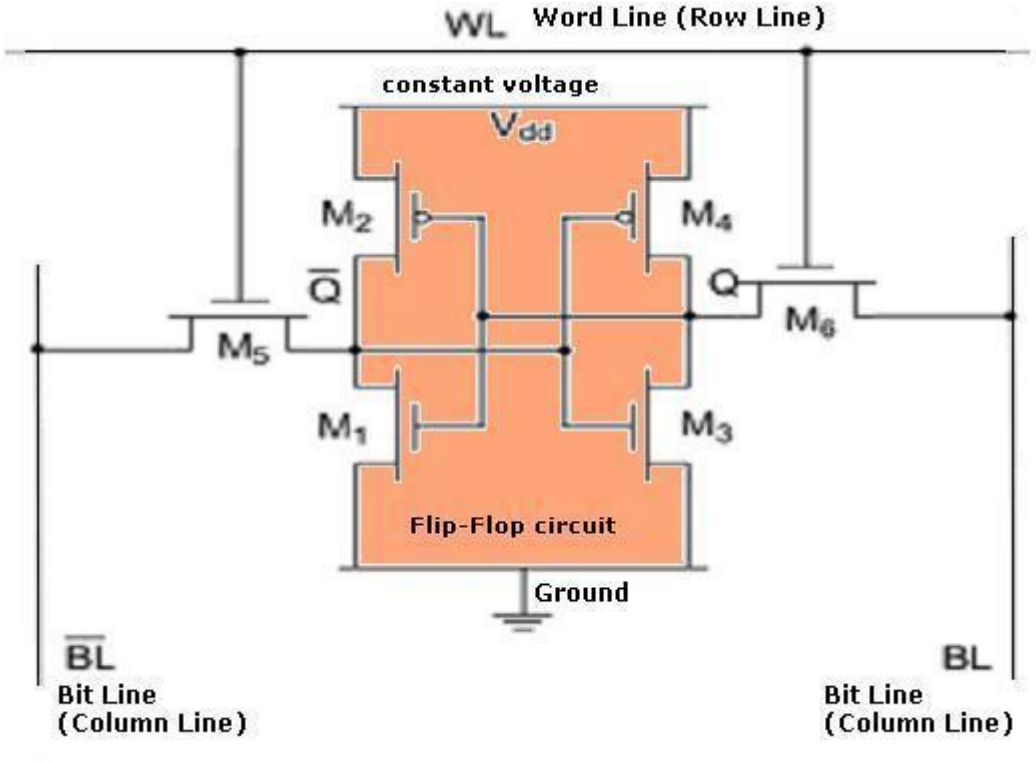
5. **Mention few applications of PLA and PAL.**

- Implement combinational circuits
- Implement sequential circuits
- Code converters
- Microprocessor based systems

6. **What are the different types of programmable logic devices?**

- PROM
- PLA
- PAL
- GAL

7. **Draw the structure of a static RAM cell.**



8. List the advantages of PLDs.

- low and fixed (two gate) propagation delays (typically down to 5 ns),
- simple,
- low-cost (free),
- Design tools.

9. What is PAL?

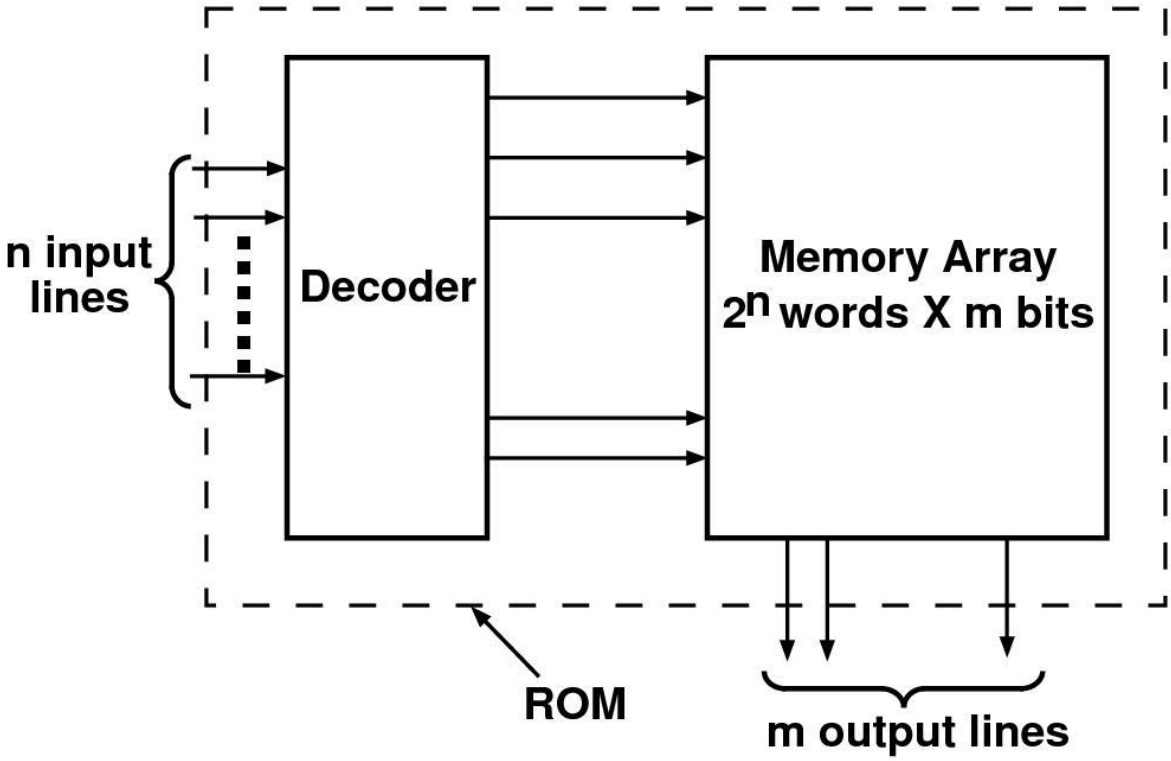
PAL is programmable array logic, PAL consists of a programmable AND array and a fixed OR array with output logic**.**

10. What is access time and cycle time of a memory?

Access time is the maximum specified time within which a valid new data is put on the data bus after an address is applied.

Cycle time is the minimum time for which an address must be held stable on the address bus in read cycle.

11. Implement a 2-bit multiplier using ROM. [Nov/Dec-2010]

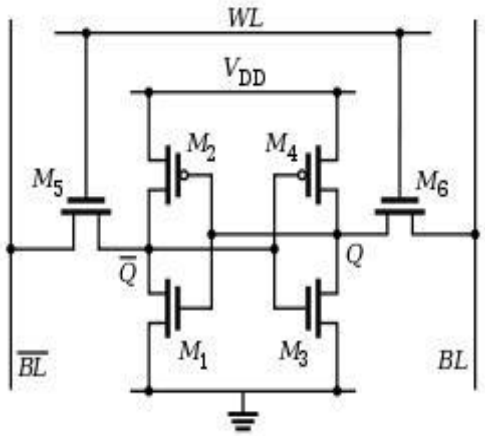


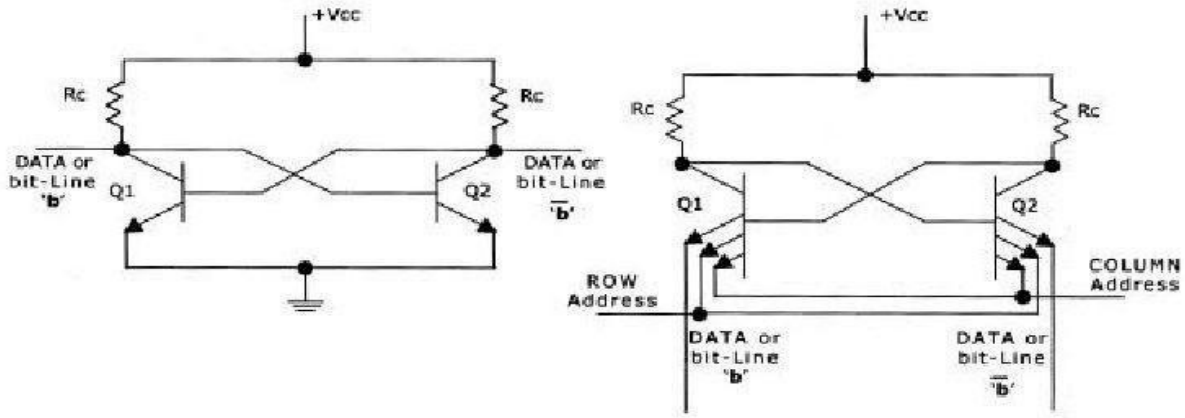
12. How the memories are classified?

It is classified into two types:

- volatile
- non-volatile memory

13. Draw the logic diagram of a static RAM cell and Bipolar cell.





14. What is volatile and non-volatile memory?

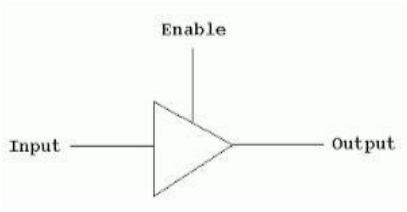
The memory which cannot hold the data when power is turned off is known as volatile memory.

The memory which can hold the data when power is turned off is known as non-volatile memory

15. Give the advantages of RAM.

- Read and write the data.
- Data is accessed by using address of the memory location.
- Higher speed.

16. **Draw an active-high tri-state buffer and write its truth table.**



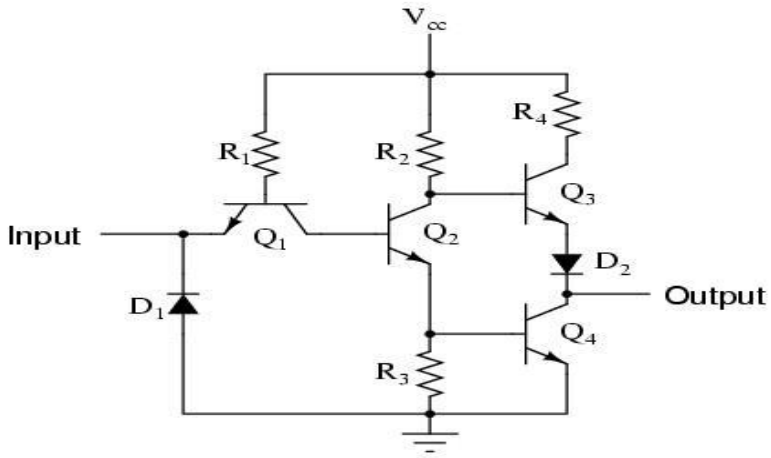
Enable	Input	Output
0	X	Z
1	0	0
1	1	1

17. What is a totem pole output?

Totem pole output is a standard output of a TTL gate. It is specifically designed to reduce the propagation delay in the circuit and to provide sufficient output power for high fan-out.

18. Draw the TTL Inverter (NOT) Circuit.

Practical inverter (NOT) circuit



19. State the advantages of CMOS logic.

- Consumes less power.
- Can be operated at high voltages, resulting in improved noise immunity.
- Fan-out is more.
- Better noise margin.

20. Write a note on tri-state gates.

It is a digital circuit that exhibits three states. Two of the states are signals equivalent to logic1 and logic 0. The third state is high impedance state. High impedance state behaves like a open circuit.

21. What is the significance of high impedance state in tri-state gates?

a. High impedance state of a three-state gate provides a special feature not available in other gates.

b. Because of this features a larger number of three state gate output can be connected with wires to form a common line without endangering loading effects.

22. Define the term Fan out.

It is the maximum number of inputs which have same family that the gate can drive maintaining its output within the specified limits.

23. Draw the CMOS inverter circuit.